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DIELECTRIC LAYERS ON III-V SEMICONDUCTORS

Annual Report: October 1979

ONR Contract N00014-76-C-0976

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by

James R. Sites

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Department of Physics

Colorado State Univeristy

Fort Collins, Colorado 80523

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Dielectric layers, particularly SiO_2, Si_3N_4, and AlN, have been deposited on GaAs and other compound seniconductors for several purposes: (1) study of MIS structures, (2) encapsulation during annealing, and (3) electronic profiling of epitoxial layers. Development of the ion beam sputtering technique has paralleled the dielectric studies.

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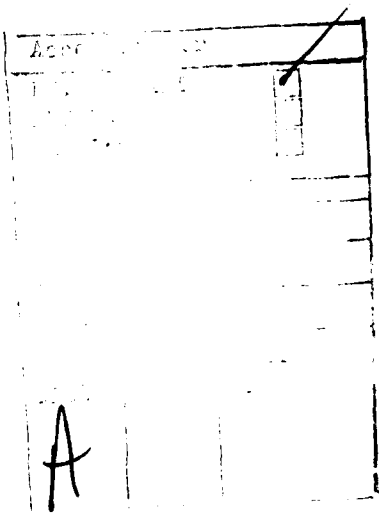

1. Introduction

The past three years have seen a rapid increase in the utilization of III-V semiconductors in such applications as heterojunction lasers, optical detectors, and field effect transistor circuitry. These applications have been paralleled by progress in synthesis, characterization, and fundamental understanding of these semiconductors and their interfaces with other materials.

Several individual projects have been completed under ONR Contract N00014-C-76-0976 in the general area of dielectric layers on III-V compound semiconductors. These investigations include: (1) metal-insulator-semiconductors (MIS) structures on GaAs, (2) encapsulation of GaAs with oxides and nitrides of silicon and aluminum for annealing purposes, and (3) electronic profiling of thin InAs layers. Additionally, there has been an evolution of new laboratory techniques, particularly those related to ion beam sputter deposition of dielectric materials. The sections that follow will describe the results form each area of study and will conclude with some general observations and suggestions for future studies. The final section will present the abstracts of reports, and in some cases the full technical reports, generated under this contract.

The research reported here has all been done in the framework of the graduate degree programs at Colorado State University. It is gratifying to acknowledge the hard work and creative thought of several students and visitors: Larry Meiners, Hudson Washburn, Ru-pin Pan, Lynn Bradley, Joe Bowden, Sung Pak, Helmut Schmidt, Phil Jensen, and Hülya Birey. Much of the work was carried out in partial collaboration

with the Naval Ocean Systems Center (NOSC) profiting from the advice and assistance of Harry Wieder, Division Leader for Electronic Materials. Finally, I would like to acknowledge the constructive interaction with the Office of Naval Research, particularly the timely feedback from Max Yoder.

2. Work Completed

2.1. GaAs MIS Structures. The original motivation for our dielectric layer program was to investigate the possibility of inverting the surface of gallium arsenide. Success would be the first step in the development of normally off logic circuitry analogous to that of silicon. When we began (1976), progress by others had led to anodic oxides on GaAs which were insulating and to some degree passivating.[1] It seemed prudent, therefore, to investigate MIS structures made with other insulators and deposition techniques.

We had found that our low energy, neutralized ion beam sputtering techniques (See Sec. 2.4) were extremely useful for exploratory studies. This type of deposition offers a high degree of flexibility including: (1) use of essentially any target materials, (2) ability to change or mix the beam constituents, (3) independent control of primary beam energy (50 - 1500eV) and intensity (0 - 2.5 ma/cm^2), as well as background pressure (2-20 X 10^{-5}torr), (4) option of predeposition sputter cleaning of target and/or substrate, and (5) control of substrate temperature from that of the laboratory environment upwards.

The two insulators we studied in the MIS configuration were tantalum oxide and silicon dioxide. An argon beam was used to sputter Ta_2O_5 and SiO_2 targets. Additionally a mixed argon/oxygen beam was used with a pure tantalum target. In general, the films produced were mechanically sound, transparent, relatively high in resistivity, fairly immune to electrical breakdown, and slightly lower in dielectric constant than reported bulk

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1. H. Hasegawa, K. E. Forward and H. L. Hartnagel, Electron. Lett. 12, 53 (1976).

values. Our ability to move the surface potential, as deduced from 1MHz capacitance-voltage (CV) measurements seemed promising, ans the initial results[2] were presented at the 4th PCSI Conference in Princeton. Of considerable interest to us was that the density of surface states extracted from the CV measurements was remarkably similar to that of structures with pyrolytically deposited SiO_2 and anodic oxidation.[3]

At this point it was realized, principally by Larry Meiners, that something was wrong with the interpretation of CV measurements on our GaAs MIS structures as well as with several results reported by others. He noted that the carrier density indicated by the 1MHz curves was inconsistent with that from Hall measurements. He also recognized that large variations in surface state density with surface potential ψ_s can lead to CV curves which are qualitatively similar to the textbook curves depicting the onset of accumulation and inversion.

To distinguish between a large number of surface states and a large number of free surface carriers (accumulation or inversion regimes), the circuit model below was considered. The surface states, of course, have a distribution of response times, τ, and hence the above picture is over-simplified. Nevertheless, the qualitative trends are valid: (1) the surface state contribution $C_s(1 + \omega^2\tau^2)^{-1}$ becomes progressively less significant for higher frequency ω, and (2) the insulator capacitance C_i (in series) becomes less important for small insulator thickness d_i. Using these observations and a great deal of careful measurement at

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2. L. G. Meiners, Ru-Pin Pan and J. R. Sites, J. Vac. Sci. Technol. 14, 961 (1977). [See Appendix A]
3. C. R. Zeisse, L. J. Messick and D. L. Lile, J. Vac. Sci. Technol. 14, 957 (1977).

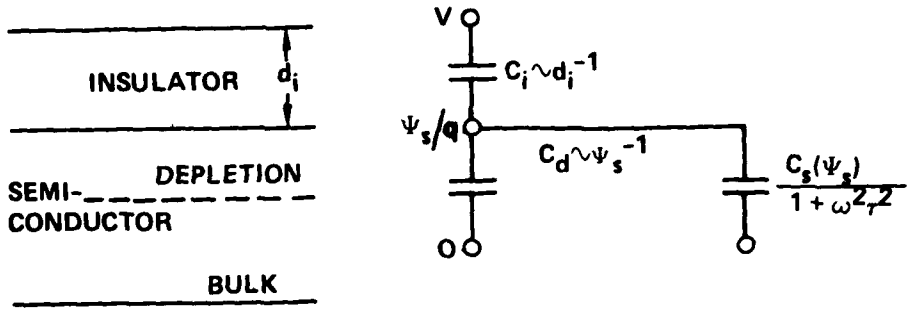

Fig. 2.1. Circuit model of MIS structure

frequencies up to 150MHz, Meiners was able to unravel the surface state distribution and the resulting dependence of surface potential Ψ_S on applied bias V for GaAs.[4-6]

The surface state densities from both n- and p-type GaAs are shown in Fig. 2.2 on the following page. In both cases depicted the insulator was formed by anodic oxidation. This analysis clearly demonstrates that the GaAs Fermi level is pinned in a region extending from approximately 0.7 to 1.1eV below the conduction band minimum. It cannot be moved outside this region with any reasonable gate bias, and the pinning to first order is independent of the insulator used or the GaAs carrier type. This result is supported by both photoemission measurements[7] and by recent theoretical calculations.[8] The inescapable conclusion is that

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4. L. G. Meiners, PhD Thesis, Colorado State Univ., Ft. collins, CO 1979. [See Appendix I]
5. L. G. Meiners, J. Vac. Sci. Technol. 15, 1402 (1978).
6. L. G. Meiners, Appl. Phys. Lett. 33, 747 (1978).
7. W. E. Spicer, I. Lindau, P. E. Gregory, C. M. Garner, P. Pianetta, and P. W. Chye, J. Vac. Sci. Technol. 13, 870 (1976).
8. J. J. Barton, W. A. Goddard III and R. C. McGill, to be published.

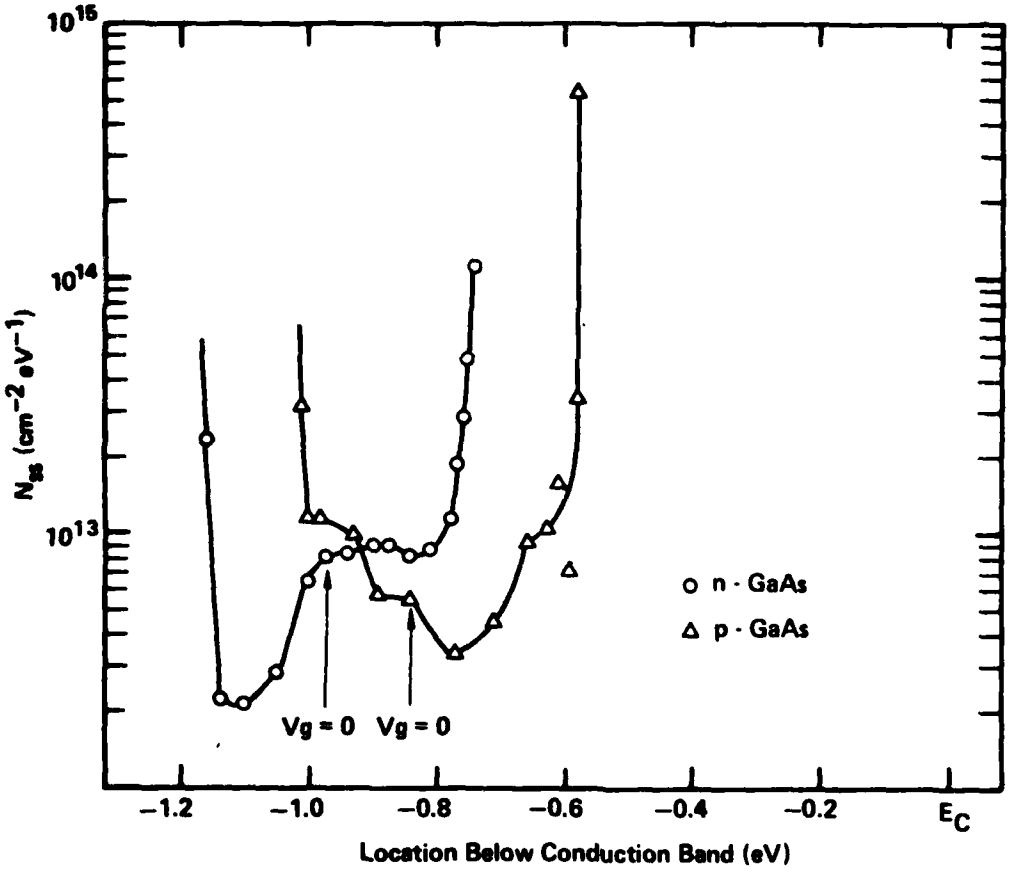

Figure 2.2 Surface state density of GaAs. [L. G. Meiners, PhD Thesis, Colorado State Univ., 1979]

the GaAs surface can be neither inverted nor accumulated nor even brought to flat band with any of a wide variety of insulators.

The situation with InP, also studied by Meiners, is considerably more hopeful.[4,9,10] Similar CV measurements over a wide range of frequencies show that the C_s contribution to the measured capacitance is much less pronounced. The surface state densities extracted from the indium phosphide measurements are plotted in Fig. 2.3. In this case the insulator is pyrolytically deposited SiO_2. In contrast to the GaAs curve, the density is lower, and remains low over a larger portion of the band gap. The implication is that it is possible to move the surface potential of InP over a large range, including the inversion condition necessary for an enhancement mode transistor.

2.2. Encapsulants on GaAs. In addition to the MIS structure, we have also deposited dielectric layers on gallium arsenide to encapsulate the surface during annealing. This procedure is particularly applicable following ion implantation when one wants to anneal out structural damage, but not lose arsenic from the surface or allow foreign constituents to diffuse in. We have deposited and tested both silicon nitride and aluminum nitride as well as their oxynitrides, for this purpose. Both nitrides were chosen for their chemical stability. Again we used the ion beam technique, taking particular advantage of the capability for room temperature deposition and the good adhesion associated with the 10 - 20eV energies of the sputtered atoms.

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4. L. G. Meiners, PhD Thesis, Colorado State Univ., Ft. Collins, CO, 1979. [See Appendix I]
9. L. G. Meiners, Thin Solid Films 56, 201 (1979).
10. L. G. Meiners, J. Vac. Sci. Technol. 16, xxxx (1979).

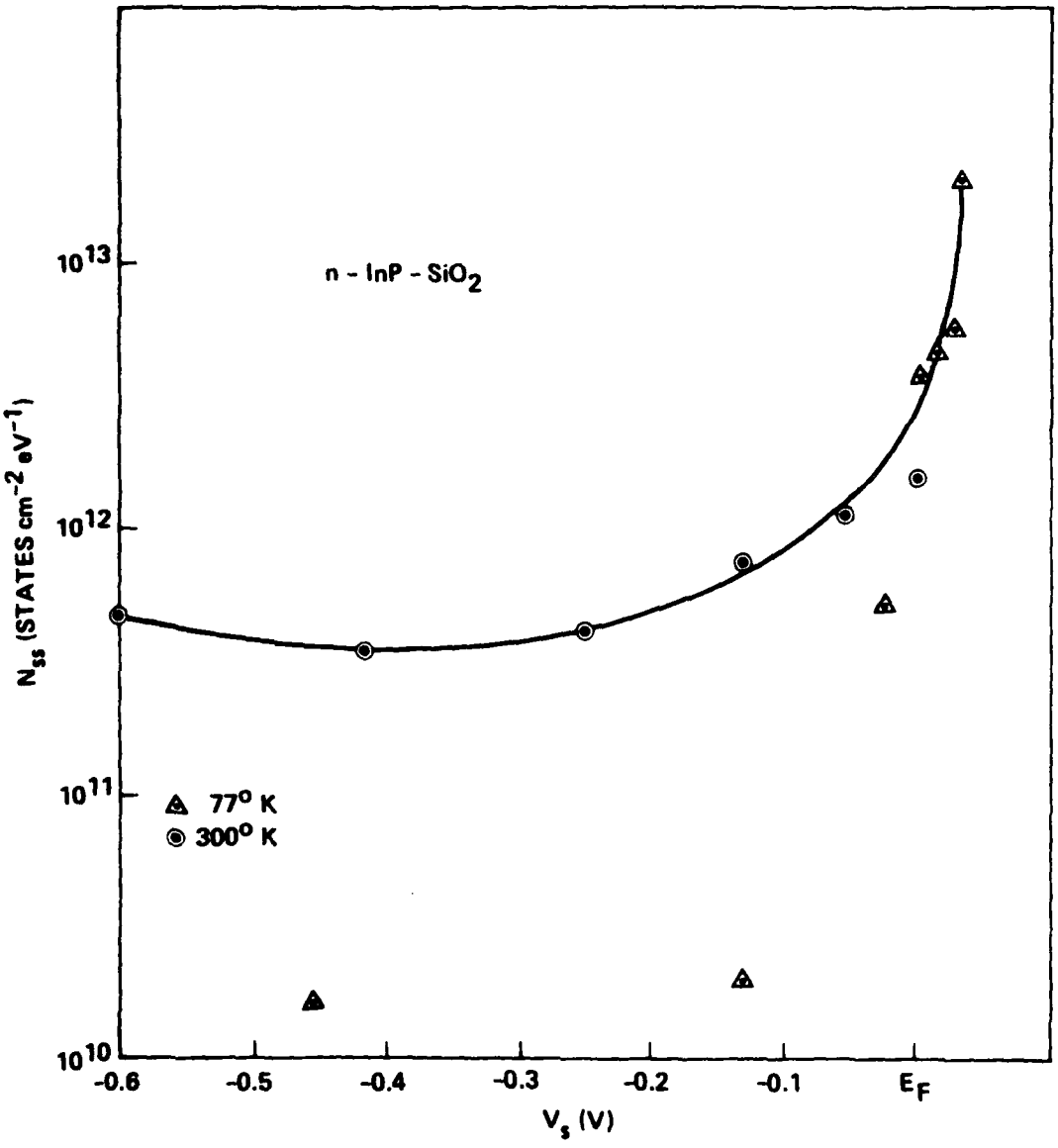

Figure 2.3 Surface state density of n-type InP coated with silicon oxide. [L. G. Meiners, PhD Thesis Colorado State Univ., 1979]

In order to evaluate the potential effectiveness of our encapsulating layers, we invoked several test procedures. Visual inspection before and after annealing, electrical and optical characterization of the films, and Auger electron spectroscopy search for diffused constituents give indications of gross difficulties with the sputtered layers. A much more sensitive evaluation, however, came from photoluminescence (PL) studies. These measurements can reveal both the loss of arsenic and the in-diffusion of impurities from the outside.

The PL apparatus we assembled [See Appendix J, Fig. 1], was designed to be straightforward, but reliable. The sample temperature could be varied from 20 to 300K, but we have done most measurements at liquid nitrogen temperature. For reference, we examined uncoated n-type gallium arsenide of several different doping concentrations, that had been subjected to various heat treatments.[11,12] The primary conclusions from this work were: (1) the near bandgap PL line increases in intensity with heating,particularly dramatically for the lightly doped material, (2) a new line at 1.36eV appears at temperatures of 600°C and above, and (3) both of these effects take place within 1μm of the surface. We attributed the heat treatment PL effects to the loss of arsenic from the surface, and we adopted the point of view that a similar change in the PL spectrum of encapsulated samples was an indicator that the encapsulant was failing. For further tests, we chose to use the lightly doped material ($\sim 10^{16} cm^{-3}$ of silicon) since it had less background spectrum to obscure surface deterioration effects.

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11. H. Birey and J. R. Sites, J. Appl. Phys. in press. [See Appendix J for full text]
12. H. Birey and J. R. Sites, unpublished. [See Appendix M]

Initial encapsulants of Si_3N_4 were deposited by using a mixed argon/nitrogen ion beam impinging on a pure silicon target.[13] These first experiments showed that the silicon nitride could be deposited without affecting the PL spectrum. With attention to general vacuum procedures and with judicious cleaning of the GaAs before deposition, the deposited layers were mechanically sound following annealing cycles in excess of 900°C. The GaAs PL spectrum, however, showed the characteristic onset of the 1.36eV line at temperatures between 500°C and 600°C. Also of interest in the early deposition was a strong correlation between the refractive index of the deposited layer and its ability to withstand high temperatures. A low index was nearly always an indicator of later trouble. [See Appendix E].

Depositions of aluminum nitride, where a high purity aluminum target was substituted for the silicon, yielded somewhat similar results.[14] As others had reported for SiO_2/Si_3N_4 comparisons, we found that the inclusion of oxygen, either purposefully or accidently, degraded the resistance of the interface to cross diffusion at elevated temperatures. We also found that the argon component of the ion beam was not essential and that nitrogen could be used as both sputter agent and reactive constituent for the deposited film.

With time we were able to reduce the oxygen content in our silicon and aluminum nitride films, and to improve their overall quality. More

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13. L. E. Bradley and J. R. Sites, J. Vac. Sci. Technol. 16, 189 (1979). [See Appendix E for full text]
14. H. Birey, S. Pak, J. R. Sites, and J. F. Wager, J. Vac. Sci. Technol., in press. [See Appendix G]

recent depositions have produced films where no PL changes in the GaAs were observed until the annealing temperature reached 800°C in the case of AlN and 900°C for Si_3N_4, significantly higher than before.[15] No other evidence of interfacial deterioration was observed.

The conclusion from the above studies is that the ion beam sputtered nitride layers are effective encapsulants and compare favorably with those fabricated by other techniques. Their utility is probably not limited to GaAs, and their integrity at high temperatures may be even more useful in the annealing of indium phosphide where the tendency to lose phospherous is even greater than that of GaAs to lose arsenic.

2.3. Profiling of InAs Epilayers. A third area of study involving a dielectric layer on a III-V semiconductor was oriented toward gate control of the surface potential in InAs and the resulting impact on the transport along an epilayer. n-type InAs was chosen because the naturally accumulated surface gave a marked contrast between surface and bulk properties and because the light effective mass was likely to lead to quaautum effects in the accumulation layer. Following earlier work,[16,17] we adopted a model in which the epilayer was divided into three regions: (1) the substrate interface, (2) the bulk of the layer, and (3) the surface accumulation layer.[18,19] The electron density of the latter can be externally controlled through application of a gate bias.

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15. H. Birey, S. Pak, and J. R. Sites, Appl. Phys. Lett. 35, 642 (1979). [See Appendix L for full text]
16. H. H. Wieder, Appl. Phys. Lett. 25, 206 (1974).
17. J. R. Sites and H. H. Wieder, CRC Crit. Rev. Solid State Sci. 5, 385 (1975).
18. H. A. Washburn, Thin Solid Films 45, 135 (1977). [See Appendix C]
19. H. A. Washburn, PhD Thesis, Colorado State Univ. (1978).

The specific epilayers studied were 5-15 μm thick, grown on semi-insulating GaAs substrates by VPE techniques at NOSC. The substrate interface was studied by successively thinning the InAs in 0.5 μm increments by ion milling. Assuming that the top surface condition is the same after each milling operation, a difference procedure allows the extraction of the carrier and scattering profiles as one approaches the substrate.[19,20] For the samples studied, we found that the density of both carriers and scattering sites increased in the neighborhood of the interface. The interfacial values were to first order independent of temperature.

The top surface of the InAs was studied by varying the surface potential with an insulated gate. In this case the insulator was pyrolytically deposited SiO_2. Although the surface potential is difficult to move, it is possible to achieve flat band by applying about 30 volts across the 1000Å dielectric. As the surface potential is varied from flat band to approximately one-half the band gap into the conduction band, the carrier density increases more-or-less linearly and the surface mobility falls from near the bulk value (40,000 cm^2/V-sec) to about one tenth that value. The shape of the decrease is consistent with the electrons being trapped in a potential well which is becoming deeper and which exhibits partially diffuse scattering from one side. As with the interfacial electrons, these also show a density and mobility which is nearly temperature independent. In contrast [See Appendix F] the bulk epilayer mobility behaves as expected with a pronounced maximum near 80°K.

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20. H. A. Washburn, J. R. Sites and H. H. Wieder, J. Appl. Phys. 50, 4872 (1979). [See Appendix F for full text]

The application of a magnetic field at temperatures of 70°K and below results in the oscillatory behavior of resistance and Hall coefficient with either magnetic field or gate voltage. These oscillations, interpreted as resulting from the quantization of the accumulation layer electrons into subbands, occur for magnetic fields of 0.5T and above and for gate voltages more positive than the flat band voltage. Three distinct subbands are discerned, each of which shows an electron density [Appendix F, Fig. 9] linear in applied gate voltage.

The fact that the oscillatory behavior extends to relatively high temperatures is indicative of a low effective mass m*. If the temperature dependence of the resistance oscillations is used to extract the average effective mass of the InAs accumulation electrons, one finds a pronounced dependence of m* on surface potential. It rises by a factor of three over that found at the conduction band minimum. Such a large rise, [Appendix F, Fig. 11], however, is consistent with the Kane model of nonparabolic bands.

The implications of this project for InAs MIS devices are that it may be difficult, though not impossible, to switch the conduction channel of InAs on and off under gate control. One must also anticipate a significantly reduced mobility and an enhanced effective mass in the surface channel as compared with bulk values.

2.4. Ion Beam Sputtering. Throughout the work described in the preceding sections, we have tried to improve and better understand the ion beam sputter deposition process.[21] Some time ago, we concluded that the

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21. For a comprehensive discussion, see J. M. E. Harper, Thin Film Processes, ed. J. L. Vossen and W. Kern (Academic Press, New York, 1978), p. 177.

low energy ion beam, where all accelerating potentials are removed from the target/substrate area and where the beam can be made into a neutral plasma by adding electrons, offered distinct advantages over other sputtering techniques. In particular we are convinced that the ability to vary the target and beam constituents, plus the stability and independence of the beam parameters provide the flexibility one should have for exploratory studies. The same apparatus can in fact produce a wide variety of thin film layers.[22] The primary drawback in our opinion is the relatively slow rate of deposition ($\sim$1μm/hour).

Our current ion beam system is an attempt to realize both clean vacuum conditions and fast turn arond time. It uses cryopumping to maintain an oil free vacuum environment. At the same time, it is equipped with hinged doors with o-ring seals for fast access to both the ion source and the target/substrate fixturing. The cryopump has served well except that it becomes somewhat unstable when hydrogen is mixed into the ion beam.

We have made considerable effort to characterize both the pumping cycle and the ion beam parameters of our specific system. The details are contained in an unpublished report [See Appendix H] available on request. We have also investigated the operation of the ion beam system when different gases and mixtures are used for the beam.[23] We find that argon, krypton, and nitrogen can be utilized with relative ease, but that oxygen shortens the life of the ion source filaments.

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22. J. R. Sites, Proc. 7th Intl Vac. Congress, Vienna, 1977, p. 1563; Thin Solid Films 45, 47 (1977). [See Appendix B]
23. S. Pak and J. R. Sites, submitted to Rev. Sci Instrum. [See Appendix N]

In order to provide good film adhesion and remove surface contamination, we have generally arranged our fixturing so that the substrates can be exposed to the ion beam for *in situ* sputter cleaning. Although low energies (100 - 500eV) are used, there has always been some question as to the extent and depth of damage caused by the sputter beam. We therefore exposed GaAs to several different argon beam energies and measured the effect on the ability to form gold Schottky barriers.[24] The conclusions were: (1) at low beam energies (50 - 100eV), there is small increase in barrier height, probably due to compensation or type conversion at the surface, (2) at beam energies between 100 and 300eV, the Schottky barrier height falls rapidly and above 300eV the contact is essentially ohmic, and (3) the thickness of GaAs that must be removed to restore the original barrier is relatively small, ranging from about 20Å for a 50eV to 50Å for 500eV.

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24. H. E. Schmidt, P. E. Jensen and J. R. Sites, submitted to Solid State Electronics. [See Appendix O]

3. Future Directions

Ion beam sputtering of dielectrics has turned out to be a valuable technique in the fabrication of new structures. This capability may well lead to one or more breakthroughs in MS/MIS technology involving III-V semiconductors. Specifically the following possibilities, some of which are interrelated, should be considered:

(1) MIS InP devices. The promise of InP in an enhancement mode structure makes it essential to find the best material and procedures for the dielectric. Low temperature plasma deposition of SiO_2 and Si_3N_4 appears to be effective, but it would be a mistake to foreclose other possibilities. A side-by-side comparison with sputtered dielectrics, particularly Si_3N_4 would seem appropriate. The net charge of the ion beam should be varied to see if trapped charge in the sputtered dielectric can be eliminated.

(2) Doping of GaAs and InP. Following the investigations of Arnold et al,[25] it seems feasible to diffuse dopants out of an encapsulating dielectric into semi-insluating material. Ion beam sputtering of the dielectric, already known to be effective for encapsulation, has the capability for careful control of the amount of dopant. Furthermore, it can be easily arranged to deposit a double layer where the dopant is concentrated right at the GaAs surface.

(3) Encapsulation of InP. Dielectrics such as Si_3N_4 and AlN should be sputtered onto InP for encapsulation purposes. At the same

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25. N. Arnold, H. Daembkes, and K. Heine, Proc. Intl. Conf. on Solid State Devices, Tokyo, September 1979.

time a relationship must be established with a laboratory which can perform a simple implanting operations on a fast turn around basis.

(4) Barriers and contacts. There are several small projects involving rectifying and ohmic contacts to compound semiconductors that should be explored. Among these is the possibility of forming higher barriers by sputtering carefully controlled mixtures onto the semiconductor. Of particular interest is n-type InAs where there has been some difficulty in obtaining a good barrier. Another project is exploring the use of ion beam sputtering for formation of ohmic contacts on troublesome materials, and still another is further investigation of the damage resulting from ion milling of semiconductor surfaces.

The primary conclusion from the work done to date is that dielectric layers, an important component of compound semiconductor technology, require careful and systematic study. Obviously, much more work needs to be done, and in our opinion, the ion beam techniques can play a significant role.

4. Reports and Publications

The technical reports listed below were generated under Contract N00014-76-C-0976. The appendices that follow reproduce the first page, and in some cases the full published versions, of the technical reports.

SF 9 (Appendix A)	"Oxide Barriers on GaAs by Neutralized Ion Beam Sputtering," by L. G. Meiners, Ru-Pin Pan, and J. R. Sites. J. Vac. Sci. Technol. 14, 961 (1977).
SF 10 (Appendix B)	"Semiconductor Applications of Thin Films Deposited by Neutralized Ion Beam Sputtering," by J. R. Sites, Thin Solid Films 45, 47 (1977).
SF 11 (Appendix C)	"Multilayer Model of Indium Arsenide Epilayers," by H. A. Washburn. Thin Solid Films 45, 135 (1977).
SF 13 (Appendix D)	"Oscillatory Transport Coefficients in InAs Surface Layers," by H. A. Washburn and J. R. Sites, Proc. EP2DS, Berchtesgaden, 1977, and Surf. Sci. 73, 135 (1978).
SF 14 (Appendix E) Full Text	"Silicon Nitride Layers on Gallium Arsenide by Low Energy Ion Beam Sputtering," by L. E. Bradley and J. R. Sites, J. Vac. Sci. Technol. 16, 189 (1979).
SF 15 (Appendix F) Full Text	"Electronic Profile of n-InAs on Semi-insulating GaAs," by H. A. Washburn, J. R. Sites, and H. H. Wieder, J. Appl. Phys. 50, 4872 (1979).
SF 17 (Appendix G)	"Ion Beam Sputtered AlO_xN_y Encapsulating Films," by Hülya Birey, Sung-Jae Pak, J. R. Sites, and J. F. Wager, J. Vac. Sci. Technol. 16, xxxx (1979).
SF 18 (Appendix H)	"Cryopumped Ion Beam Sputter Deposition System: Desciption, Operation, and Optimization," by Sung-Jae Pak, unpublished.

SF 19 (Appendix I)	"Dielectric-Semiconductor Interfaces of GaAs and InP," by Larry G. Meiners, PhD Thesis, Colorado State Univ., 1979.
SF 20 (Appendix J) Full Text	"Radiative Transitions Induced in Gallium Arsenide by Modest Heat Treatment," by Hülya Birey and James Sites, J. Appl. Phys., in press.
SF 21 (Appendix K)	"Thickness and Refractive Index of Thin Transparent Films by Spectrophotometric Transmissivity," by Hülya Birey, unpublished.
SF 22 (Appendix L) Full Text	"Photoluminescence of Gallium Arsenide Encapsulated with Aluminum Nitride and Silicon Nitride," by Hülya Birey, Sung-Jae Pak, and J. R. Sites, Appl. Phys. Lett. 35, 623 (1979).
SF 23 (Appendix M)	"Depth and Carrier Concentration Dependence of Photoluminescence Features in Heat Treated GaAs:Si," by Hülya Birey and James Sites, unpublished.
SF 24 (Appendix N)	"Broad Beam Ion Source Operation with Four Common Gases," by S. Pak and J. R. Sites, submitted to Rev. Sci. Instrum.
SF 26 (Appendix O)	"Sputter Damage in GaAs Exposed to Low Energy Argon Ions," by H. E. Schmidt, P. E. Jensen, and J. R. Sites, submitted to Electronic Letters.

Reprinted from

APPENDIX A

Journal of Vacuum Science & Technology

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July/August 1977

Oxide barriers on GaAs by neutralized ion-beam sputtering[a)]

L. G. Meiners,[b] Ru-Pin Pan, and J. R. Sites

Department of Physics, Colorado State University, Fort Collins, Colorado 80523

(Received 10 February 1977; accepted 12 April 1977)

Tantalum and silicon oxides have been sputter deposited onto gallium arsenide using a 500-eV beam of neutralized argon atoms. MIS devices show very low leakage and capacitances that can be varied from full accumulation to depletion with the application of modest voltages. Other measurements (breakdown field, dielectric constant, adherence, Auger profile, and photoluminescence) also suggest that these structures hold potential usefulness for insulated-gate GaAs circuitry.

PACS numbers: 73.40.Qv, 81.15.Cd, 85.30.Hi

INTRODUCTION

The problem of preparing an insulating layer on gallium arsenide with properties suitable for a technologically viable MIS device has proven elusive. One important constraint on the fabrication of such devices is to keep the GaAs temperature below 750°C (Centigrade) to avoid formation of arsenic vacancies at the interface.[1] Thus, limitations are placed on both the fabrication temperature and any subsequent annealing cycles. Other constraints, if one can extrapolate from the more well-understood Si-SiO_2 system, are that the chemical bonding must be strong and the impurity level low at the semiconductor–insulator interface.

Thermal oxides grown on GaAs have generally been too conductive to form an insulating barrier.[2] Anodically grown oxides[3] have good insulating properties, but have exhibited a substantial degree of charge trapping in the interfacial region. The microscopic nature of oxides grown in an aqueous environment and the effects of this environment have not yet been determined. Foster and Swartz[4] have grown silicon nitride layers by chemical vapor deposition (CVD) which also had good insulating properties, but some charge trapping at the interface.

Plasma techniques for the growth and deposition of insulating layers on the III–V compounds provide interesting possibilities. Chang and Sinha[5] have recently demonstrated growth of an oxide on GaAs using an oxygen plasma. This oxide is somewhat conductive, but the interfacial properties look relatively good. Rf sputter deposition of Si_3N_4 on GaAs has been reported as far back as 1967.[6] The requirements of forming an insulating layer with high density and low interfacial charge seemed, however, to be mutually incompatible with this technique. Quite possibly the interfacial charge results from the large amount of ion bombardment inherent to the diode rf sputtering system.

The present paper describes the application of a relatively new plasma technique for deposition of insulating layers. A beam of low-energy argon ions is neutralized by passing it by a hot filament. The resulting plasma is used to sputter insulating materials without problems of charge buildup on either the target or the substrate.

FABRICATION PROCEDURE

The sputtering arrangement is shown schematically in Fig. 1. The neutralized ion beam was produced by a 10-cm diam Kaufman-type source[7] supplied by Ion Tech, Inc. A bell jar pressure of $\sim 3 \times 10^{-4}$ Torr (4×10^{-2} Pa) argon was required to sustain the beam. Its energy can be varied from 100 to 800 eV/ion, and its current density from 0 to 2 mA/cm^2.

The gallium arsenide substrates used were Si-doped wafers ($n = 1 \times 10^{18}$ cm^{-3}) with either ⟨100⟩ or ⟨111⟩ orientation. These were mounted on a moveable platform to facilitate predeposition cleaning. In position A (Fig. 1), the beam falls on the target, sputtering away the top layer, but these sputtered particles are shielded from the substrate. In position B, the substrate is cleaned using a reduced energy beam (100 eV, 0.2 mA/cm^2) for about 5 min, being mindful of possible sputter damage discussed below.

Actual sputtering takes place in position C. The angles and positions of the substrate and target are designed to give reasonably uniform coverage and still deep the substrate out of the beam path. Using 500-eV argon ions with a density of 1 mA/cm^2, the deposition rates were approximately 40 Å/min for tantalum oxide sputtered from the metal, 10 Å/min when sputtered from Ta_2O_5 powder, and 30 Å/min for the silicon oxide sputtered from quartz. Final thickness ranged from 600 to 1800 Å. The substrate could be heated during deposition, but doing so generally produced inferior results.

As with other ion-beam sputtered films,[8] we found the

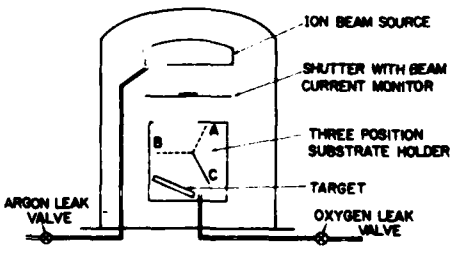

FIG. 1. Schematic of sputtering apparatus.

APPENDIX B

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SEMICONDUCTOR APPLICATIONS OF THIN FILMS DEPOSITED BY NEUTRALIZED ION BEAM SPUTTERING*

JAMES R. SITES
Physics Department, Colorado State University, Fort Collins, Colo. 80523 (U.S.A.)
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Thin films deposited by sputtering with a neutralized ion beam source have shown promise for performance improvement in two distinct types of devices: insulating barriers on gallium arsenide and heterojunction solar cells. The source, first developed by NASA for space propulsion, accelerates positive argon ions to 100–800 eV and then neutralizes the beam with electrons from a hot filament. MIS structures formed from tantalum oxide, silicon oxide and silicon nitride on GaAs show very high resistivity and relatively low surface state densities. Indium tin oxides deposited on silicon produce respectable diodes and solar cells with efficiencies as high as 12%.

1. INTRODUCTION

The use of accelerated ions for sputtering applications has evolved considerably through the years. Refinements to the d.c. glow discharge source of ions have included (a) injection of electrons, (b) magnetic containment of electrons, (c) high frequency operation and (d) neutralization of the resultant ion beam. Neutralization in this context means that sufficient electrons are added to achieve electrical neutrality; it does not imply that one has a beam of ground state atoms. The neutralization accomplishes two things: it lessens the tendency of a collimated beam to diverge, and more importantly it removes all macroscopic electric fields from the interaction of the beam with a target and from any sputtered material impinging on a substrate.

The Kaufman thruster, designed for spacecraft propulsion[1], is particularly adaptable to providing a neutralized ion beam. Such a beam has proved useful for high resolution pattern etching[2,3], surface texturing[4,5] and thin film deposition[6–8]. The neutralization step seems particularly important in semiconductor device fabrication where difficulties may arise in forming a good quality homogeneous layer when charge is present on the substrate or where charge trapping at an interface may adversely affect device operation. The neutralized ion beam also allows sputtering from essentially any type of target without special preparation and also independent control of all process parameters.

* Paper presented at the International Conference on Metallurgical Coatings, San Francisco, California, U.S.A., March 28–April 1, 1977

APPENDIX C

Thin Solid Films, 45 (1977) 135–140

MULTILAYER MODEL OF INDIUM ARSENIDE EPILAYERS*

H. A. WASHBURN
Physics Department, Colorado State University, Fort Collins, Colo. 80523 (U.S.A.)
(Received March 31, 1977; accepted March 31, 1977)

The charge carrier transport coefficients of an inhomogeneous thin semiconductor in a MOS structure were obtained using a multilayer model. The expression for the Hall coefficient of a three-layer system extended to arbitrary strength magnetic fields was used to separate the bulk transport parameters from the parameters describing transport at the two surfaces. Experimentally, a gate voltage was used to vary the surface under the oxide from depletion to accumulation, and the Hall coefficient was measured as a function of magnetic field. The characteristics of the back surface were obtained with the front surface held at the flat-band condition. The variation of the front surface parameters with gate voltage was obtained with the front surface in accumulation. The measurements were made on a MOS structure consisting of an InAs epilayer deposited by vapor phase epitaxy procedures on a semi-insulating GaAs substrate covered by a pyrolytic silicon dioxide insulating layer and an aluminum gate.

1. INTRODUCTION

InAs epilayers grown by vapor phase epitaxy (VPE) procedures on semi-insulating GaAs substrates have exhibited nearly bulk-like electrical characteristics[1–3] even though there is about a 7% lattice mismatch between the two materials and the front surface, whether free[3] or covered with an oxide[2], is normally accumulated. The InAs–GaAs interface has been shown to have a compositionally graded region[4], and the front surface is thought to contain a combination of fast and slow surface states[5]. It is thus expected that the carrier density and mobility in the epilayers will exhibit spatial inhomogeneities in a direction perpendicular to the film.

In order to understand the electrical transport in these epilayers and the influence of spatial inhomogeneities, a model of the epilayer is presented (see Fig. 1(c)) which assumes three parallel non-interacting layers: a region with bulk-like properties bounded by a front surface layer (surface 1) and an interface layer (surface 2). The magnetic field dependence of the Hall coefficient calculated for this model, when combined with gate voltage control of surface 1 from accumulation

*Paper presented at the International Conference on Metallurgical Coatings, San Francisco, California, U.S.A., March 28–April 1, 1977.

APPENDIX D

Surface Science 73 (1978) 537–544

OSCILLATORY TRANSPORT COEFFICIENTS IN InAs SURFACE LAYERS

H.A. WASHBURN and J.R. SITES
Department of Physics, Colorado State University, Fort Collins, Colorado 80523, USA

The resistivity and Hall coefficient of gated n-InAs epilayers have been measured at low temperatures utilizing differential techniques and a magnetic field swept from zero to six tesla. When the InAs surface is in accumulation, three distinct series of oscillations, periodic in inverse magnetic field, are observed. These series are interpreted as the quantization of the surface electron energies into three subbands. The densities of these subbands are roughly linear in applied gate voltage and vanish as one approaches flatband. The temperature and magnetic field dependences of the oscillation amplitudes suggests an effective mass of 0.04 m_e and a Dingle temperature of 26 K.

1. Introduction

Most surface quantization studies to date have been undertaken on inversion layers [1] in which case the surface transport can be isolated from that in the bulk. Accumulation layer transport studies have been less common. Tsui [2,3] however, has demonstrated the existence of surface quantization and characterized the behavior of the electronic energy levels in InAs surface accumulation layers using capacitance measurements and tunneling through a native oxide. At least qualitative agreement with several of the theoretical predictions of Baraff and Appelbaum [4] was found. Surface quantization in n-channel InAs inversion layers has been studied by Kawaji and Kawaguchi [5] who found an increase in mobility with carrier density, consistent with coulomb scattering in the quantized surface channel.

In this paper, we report on electrical transport measurements made on accumulation layers formed at the surface of InAs epitaxial films. To distinguish the surface contribution to the transport coefficients an MOS structure was employed and an excitation voltage was added to the dc gate voltage. The resulting differential signal was measured for both conductivity and Hall configurations as functions of gate voltage, magnetic field, and temperature. Three series of oscillations are observed and an analysis in terms of surface quantization in the accumulation layer yields information on the carrier effective mass and scattering lifetime which is compared to the bulk and surface parameters observed by others.

2. Experimental

The films of n-type InAs grown heteroepitaxially on GaAs have been described previously [6]. They are approximately 15 μm thick. Electrical measurements at

APPENDIX E

Silicon nitride layers on gallium arsenide by low-energy ion beam sputtering

L. E. Bradley[a] and J. R. Sites

Department of Physics, Colorado State University, Fort Collins, Colorado, 80523

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Silicon nitride layers are formed on gallium arsenide for encapsulation purposes. The process utilizes a 500-eV neutralized ion beam containing argon for sputtering and nitrogen for reactive deposition, directed at a pure silicon target. It is found that, with proper surface preparation, layers having mechanical stability to above 900°C can be formed. Photoluminescence shows that no radiative transitions are introduced in the deposition process, but that annealing inevitably leads to diffusion of silicon into the GaAs. Auger studies reveal significant oxygen impurity in the Si_3N_4, particularly near the interface. Index of refraction was found to be a sensitive, nondestructive test of encapsulant quality.

PACS numbers: 73.40.Qv, 73.60.Hy, 81.15.Cd

I. INTRODUCTION

Silicon nitride has been used extensively as an encapsulant to prevent loss of arsenic when gallium arsenide is thermally annealed following ion implantation. Several techniques have been employed for the deposition of the silicon nitride layers: (1) pyrolytic or chemical vapor deposition[1–4] generally involving silane and ammonia in a nitrogen carrier gas; (2) rf plasma deposition[5,6] using nitrogen and silane; and (3) rf sputtering[7,8] with a silicon target in a 100% nitrogen atmosphere. A comparison of these techniques is found in a recent review article.[9] In general, it is concluded that Si_3N_4 layers are superior to SiO_2 and other materials for encapsulation of gallium arsenide.

In the work reported here, we have utilized low energy ion beam sputtering to deposit silicon nitride. This technique has the potential advantages of room temperature deposition and a high degree of process control.

II. EXPERIMENTAL

Deposition of the silicon nitride layers was accomplished by low energy ion beam sputtering using a pure silicon target and a 2½-cm-diam beam of argon and nitrogen ions neutralized with electrons from a hot wire filament. Details of the ion beam process have been reported elsewhere.[10,11]

A stringent chemical cleaning procedure for the GaAs substrates was necessary to assure clean and reproducible surfaces. One-centimeter-square substrates cut from ⟨100⟩ GaAs purchased from Morgan Semiconductor were initially cleaned and degreased in detergent, acetone, methanol, xylene and deionized water. Next, each was dipped in 45% hot KOH by volume for 30 s for oxide removal and mounted on a polishing puck for chemomechanical polishing with a Pellon pad soaked with 1% Bromine–methanol. Each substrate was screened under the 200× magnification dark field of our microscope for scratches and etch pits.

The substrates used were dipped in 50% HCl for final oxide removal, rinsed, dried, and immediately mounted in the vacuum system. During evacuation, typically to 5×10^{-7} Torr, the ion source filaments were degassed with currents slightly greater than operating conditions. The argon necessary to start the ion beam was about 1×10^{-4} Torr. Initially a 500-eV Ar beam was used to sputter clean the target, a 3-in. Monsanto silicon wafer, for ten minutes. Next, the GaAs substrate, in most instances, was sputter cleaned. Finally, deposition itself utilized a 1 mA cm^{-2}, 500-eV beam.

The amount of nitrogen added to the 1.3×10^{-4} Torr partial pressure of argon was determined, as shown in Fig. 1, by forming layers with a wide range of nitrogen pressures. The change from a silver metallic appearance for nearly pure silicon films to the blue characteristic of transparent films in the 800-Å thickness range occurred at relatively low nitrogen gas concentrations. However, the index of refraction, which was measured at 6328 Å with a Gaertner ellipsometer, continued to decline. For a nitrogen to argon gas pressure ratio greater than 3, we found a saturation in the index of refraction of the films. This saturation was interpreted as an indication of the proper gas ratio for Si_3N_4.

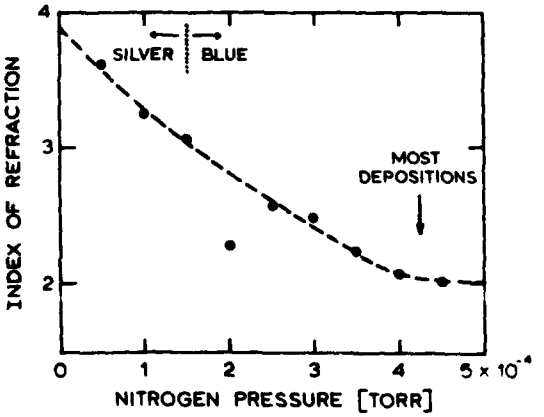

FIG. 1. *Index of refraction and color of deposited layers as a function of nitrogen partial pressure in the bell jar.*

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TABLE I. Five classes of silicon nitride layers on GaAs substrates reflecting the effects of substrate and deposition parameters on encapsulating qualities.

Class	Chemical etching	Vacuum system and pumping	Sputter cleaning	Index of refraction	Mechanical adhesion
1	no	quick pumpdown	no	1.77	poor
2	yes	first run	yes	1.89 ± .08	poor
3	no	good	yes	1.94 ± .02	poor
4	yes	good	no	2.03 ± .03	good
5	yes	good	yes	2.02 ± .03	good

Postdeposition annealing of the silicon nitride encapsulating layers was conducted in a quartz tube surrounded by resistive heating coils and continually flushed with hydrogen from a high quality generator. A maximum of 30 min was needed for the anneal temperature to be reached after which the substrates were maintained at temperature for 45 min. The system was then allowed to cool to room temperature. Typical anneal temperatures ranged from 600°–950°C.

Compositional depth profiles of the silicon nitride layers were made with a Physical Electronics Auger thin film analyzer operating with a 3-kV primary electron beam. Photoluminescence studies utilized a standard setup in which the excitation radiation was the chopped beam of a 7-mW helium–neon laser, and the emitted radiation was passed through a Jarrel-Ash ½-m spectrometer to a p–i–n detector. The current output was converted to a voltage which became the input to a lockin amplifier. In general, the sample under study was held at 20 K.

III. RESULTS

The most important parameter in determining the encapsulating quality of the silicon nitride layers is the predeposition substrate preparation procedure, including general cleanliness of the vacuum system. This point is illustrated in Table I where a total of 17 samples are grouped into five classes.

Class one is characteristic of a quick deposition. A substrate is not chemomechanically etched, the deposition chamber is evacuated only to the 10^{-6} Torr range, and there is no substrate sputter cleaning. These parameters resulted in a very low index of refraction of 1.77, and upon annealing to 700°C, the silicon nitride showed poor adhesion.

A class two sample was typically the first sample deposited after having the deposition chamber opened to air for repairs or cleaning. The adsorbed gases and contaminants were probably not fully pumped from the system prior to deposition. The substrates were chemomechanically cleaned, pumpdown was to the 10^{-7} Torr range, and one of a variety of sputter etches was conducted. These samples had a wide range of indexes and lost adhesion anywhere from 600° to 900°C. Figure 2(b) shows the affect of annealing to 600°C as compared to the pre-annealed silicon nitride surface [Fig. 2(a)]. Poor mechanical adhesion results in circular holes completely covering the sample following a single anneal. It does not appear to be a gradual process.

A clean system, pumpdown to below 5×10^{-7} Torr, and proper degassing is characteristic of class three, but the samples are not chemomechanically etched. Their indices of refraction were 1.93 to 1.96, and they degraded in the 700° to

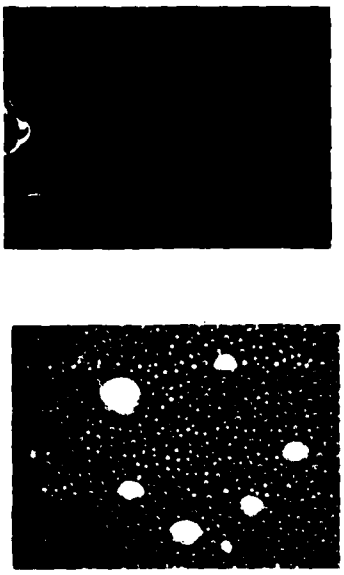

FIG. 2. Surface of sample deposited before vacuum system had been thoroughly cleaned: (a) as deposited, (b) after 600°C anneal.

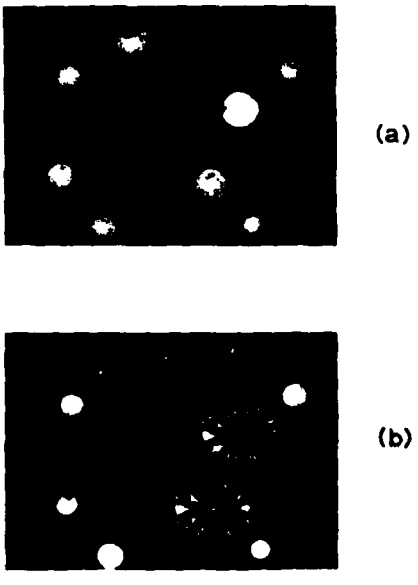

FIG. 3. Two stages of silicon nitride degradation for sample without bromine methanol treatment: (a) after 800°C anneal, (b) after 900°C.

APPENDIX E

800°C range. Figure 3(b) shows the effects of further heat treatment to 900°C after the initial degradation at 800°C shown in Fig. 3(a). The exposed GaAs has been thermally etched forming rectangular etch pits typical of ⟨100⟩ GaAs.

Class four samples were the first to display good resistance to annealing. They were chemomechanically cleaned and the vacuum system was properly pumped and degassed, but the samples were not sputter cleaned. The refractive index was about 2.03, whereas crystalline Si_3N_4 is reported to be 2.1.[12] Anneals to 900°C resulted in only very small etch pits from pinholes in the silicon nitride layer.

The last class is similar to class four except some kind of sputter cleaning was used. The index was much like class four and the samples repeatedly withstood annealing. Above 850°C, tiny etch pits were visible when viewed with the dark field of the microscope. The concentration of etch pits increased when the annealing was done at higher temperatures. Figure 4(b) shows the surface condition after annealing to 935°C, again in contrast [Fig. 4(a)] to the pre-annealed surface.

The sputter cleanings studied were combinations of nitrogen versus argon and 100 vs 500 eV. Although little difference in annealing behavior was found, it was felt that 100 eV nitrogen was not as effective and that 500-eV argon was superior but perhaps results in significant surface damage (~80 Å) to the GaAs.[13] There is some evidence[14] that a 100-eV argon beam sputters the surface stoichiometrically with only a few atomic layers of damage, but further work in this area should be done.

Turning now to the effects of deposition and annealing on the Si_3N_4/GaAs structures, we find that the Auger profiles before annealing are essentially as shown in Fig. 5 for both the class three and five samples pictured in Figs. 3 and 4. The

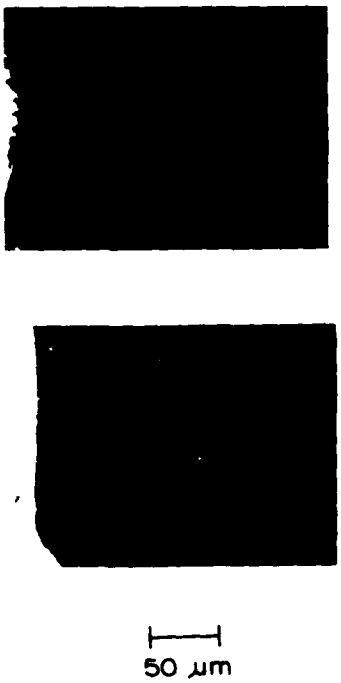

FIG. 4. Surface of sample with chemical and sputter etch substrate preparation: (a) as deposited, (b) after 935°C anneal.

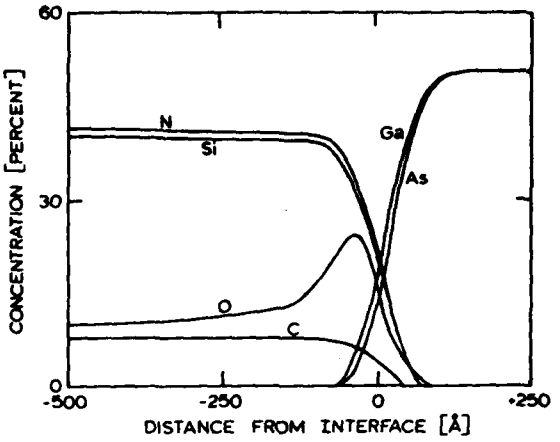

FIG. 5. Auger profile of typical sample.

important features revealed by these studies are (1) the oxygen impurity level is relatively high, as it seems to be in other processes for depositing silicon nitride; (2) there is a particularly high concentration of oxygen close to the interface with the substrate, most likely due to partial oxidation between sputter cleaning and deposition; (3) the carbon seen is probably from the grids of the ion source and can be minimized by better alignment.

Photoluminescence studies are used to detect any radiative transition processes introduced in the GaAs during either deposition or annealing. The virgin substrate before deposition (Fig. 6) shows only exiton recombination and that due to shallow carbon acceptors. The deposition process itself (middle

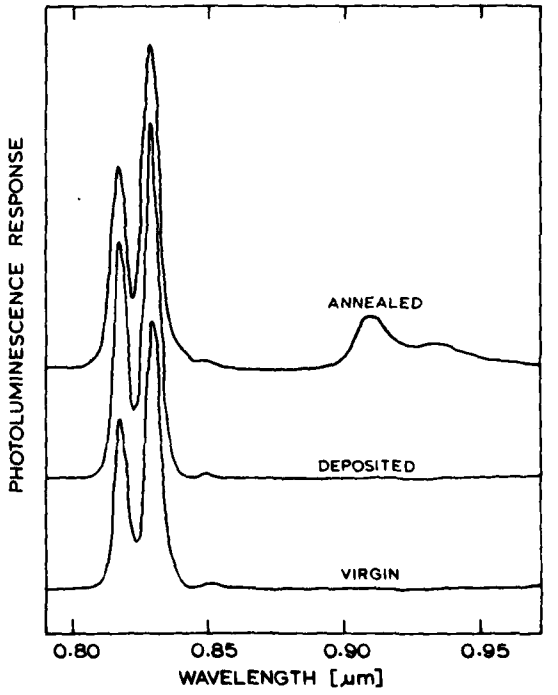

FIG. 6. Photoluminescence spectrum of 1.3×10^{17} cm^{-3} Te-doped GaAs before deposition, after deposition, and after 800°C anneal.

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curve) does not add any radiative transitions. The annealing cycles, however, even as low as 600°C, introduces the double peak structure shown. The larger peak has been previously attributed[15] to a complex between a gallium vacancy and a silicon impurity on an arsenic site, the smaller peak to the associated phonon replica. Thus, we find that even relatively modest annealing with silicon nitride encapsulants leads to a diffusion of silicon impurities into the GaAs.

IV. CONCLUSIONS

Our primary conclusion is that with reasonable care, ion beam sputtering can be used for mechanically stable silicon nitride encapsulation of gallium arsenide. There is an unexplained difficulty with excess oxygen at the interface, and there is a serious problem if diffusion of silicon dopants into the GaAs are undesirable. The latter difficulty is likely common to all deposition techniques for silicon nitride, and possibly also SiO_2, on gallium arsenide.

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[a]Present address: Loveland Instrument Division, Hewlett-Packard Company, Loveland, CO 80537.

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APPENDIX F

Electronic profile of *n*-InAs on semi-insulating GaAs

H. A. Washburn,[a] J. R. Sites, and H. H. Wieder[b]
Department of Physics, Colorado State University, Fort Collins, Colorado 80523

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The electron density and mobility of VPE-grown 15-μm *n*-type indium arsenide epilayers have been determined as a function of distance from the gallium arsenide substrate. Both epilayer surfaces show significant increases in density and decreases in mobility from the bulk values (10^{15}–10^{16} cm^{-3} and 10^5 cm^2/V sec at 77°K). The interfacial, or back, surface is apparently dominated by defects to a depth of about 3 μm. The density and mobility profiles are roughly exponential; integrated values are 1.6×10^{13} cm^{-2} and 2×10^3 cm^2/V sec. The front surface, highly dependent on applied gate bias, has a density range in accumulation from zero to 5×10^{12} cm^{-2} and mobility from 2.5×10^4 to 3×10^3 cm^2/V sec. The parameters for both surfaces are essentially temperature independent below 80°K. The front-surface effective mass increases with electron density from its band-edge value of $0.0215m_e$ to nearly $0.06\,m_e$.

PACS numbers: 73.60.Fw, 72.20.My, 73.25. + i, 73.40.Qv

I. INTRODUCTION

Many semiconductor applications utilize a conductive epitaxial layer deposited on a high-resistance substrate. In general, the electronic depth profile of such an epilayer is not homogeneous, and it may be misleading to characterize the layer with average electronic parameters such as carrier density, mobility, and effective mass. Furthermore, when one has heteroepitaxy, different materials for the substrate and epilayers, there are additional complications due to inhomogeneities in composition and defect density at the interface. Finally, when the epitaxial layer consists of a high-mobility low-effective-mass material, it may well be necessary to evaluate the effects of quantization of the surface carriers.

The purpose of this paper is to evaluate the inhomogeneities normal to the surface of high-mobility *n*-type indium arsenide layers grown on semi-insulating gallium arsenide substrates. Through a variety of measurements, primarily electrical and galvanomagnetic, we have been able to obtain (1) a profile of the electron density and mobility at the epilayer-substrate interface, (2) the bulklike properties of the main portion of the epilayer, and (3) the density, mobility, effective mass, and quantization effects of electrons in the surface accumulation layer.

II. SAMPLE PREPARATION

InAs epilayers were deposited on ⟨100⟩-oriented semi-insulating GaAs substrates by means of an open-tube chemical vapor-phase disproportionation process.[1–3] Gaseous AsH_3, HCl, and H_2 were transported at essentially constant (slightly larger than atmospheric) pressure along a quartz reaction chamber placed within a three-zone temperature-controlled furnace. Inside the chamber, the indium source material, present in the high-temperature zone, reacts with HCl. The gaseous reaction products are transported through the second intermediate-temperature zone to the low-temperature zone where they disproportionate and are deposited in the form of a single-crystal InAs layer upon the GaAs substrates.

The lattice-constant mismatch and the difference in the thermal-expansion coefficients of InAs and GaAs prevent the outright deposition and growth of high-quality epilayers. For this reason, a compositionally graded ternary $In_xGa_{1-x}As$ intermediate layer is grown upon the substrate with the grading adjusted to provide an appropriate match to GaAs at one face and to InAs at the other. This compositional grading can relieve much of the strain associated with the interfacial mismatch. InAs epilayers of thickness $d > 10\,\mu$m grown in this manner have a relatively low defect density, a low residual impurity density, and a bulk mobility which approaches theoretically calculated values, based on scattering from ionized impurities and longitudinal-optical phonons. Since the compositionally graded region perturbs electrical and galvanomagnetic measurements, it is desirable to keep the thickness of the compositionally graded region as small as practical without sacrificing the crystalline perfection. Fortunately, this can be done by means of relatively simple empirical procedures which require an appropriate choice of the temperature of each reactor zone, the temperature gradients between them, the partial pressures of the constituents, and the gas flow rates. In this manner the thickness of the interfacial region can be kept to the order of or less than 1 μm.

The samples described below were grown to thicknesses in the range between 10 and 15 μm. The metal-insulator-semiconductor (MIS) structures shown in Figs. 1(a) and 1(b) were made by photolithographic procedures; undesired portions of the InAs epilayers were removed by etching while retaining the portions protected by photoresist. An SiO_2 insulating layer ($\sim$0.15 μm thick) was deposited by the low-temperature pyrolysis of silane on the clean InAs surfaces. Finally, Ni gate electrodes [shaded area of Figs. 1(a) and 1(b), typically 3–10 mm^2] were deposited and leads attached to the electrodes.

The cross sections of the complete devices are shown in Fig. 1(c), which also shows schematically three regions of

[a] Present address: Intel Magnetics, Santa Clara, Calif. 95051.
[b] Permanent address: Electronic Materials Sciences Div., NOSC, San Diego, Calif. 92152.

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APPENDIX F

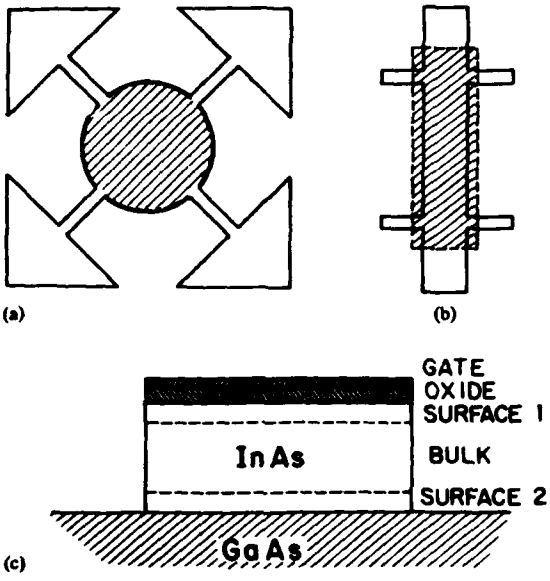

FIG. 1. (a) Sample configuration referred to as the cloverleaf. (b) Bridge-shaped sample configuration. (c) Cross section of InAs MOS structure.

the epilayer: Surface 1 is a region characterized by electron accumulation; the bulk region is characterized by properties very similar to those of bulk single-crystal n-type InAs; and surface 2 is the interfacial region adjacent to the semi-insulating GaAs substrate.

III. MEASUREMENT

For most of the electronic measurements described in this paper the indium arsenide MIS structures were mounted in the variable-temperature bore of a superconducting magnet. The sample temperature could be varied from 1.6 to 400 °K and the transverse magnetic field from 0 to 6 T. The apparatus used for dc conductivity and Hall measurements is shown schematically in Fig. 2(a). For clarity only two switch positions are shown; the other two switch positions are used for permutations of contacts. The currents used were 0.1 or 1.0 mA; these currents do not produce any significant Joule heating of the sample. For some measurements, particularly those involving the thickness dependence of the electrical and galvanomagnetic properties of the epilayers, the gate contact was omitted.

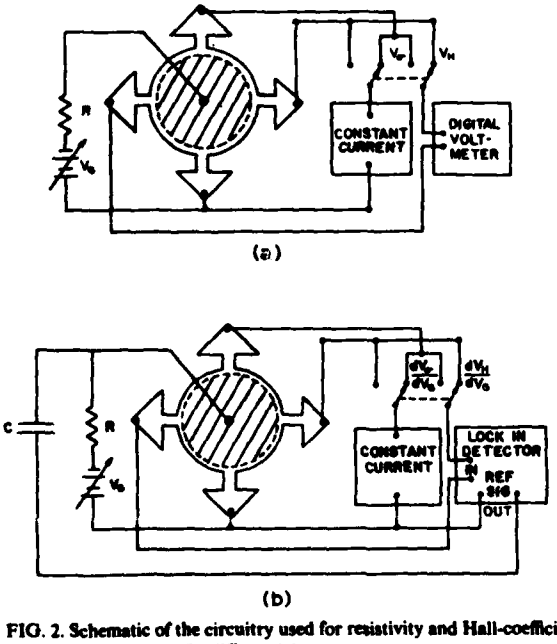

FIG. 2. Schematic of the circuitry used for resistivity and Hall-coefficient measurements; (a) dc, (b) differential.

FIG. 3. SEM photograph showing contrast in texture between indium arsenide (right) and gallium arsenide (left) when both are exposed to 500-eV ion milling. Region shown is $60 \times 80\ \mu$m.

The ac, or differential, mode used in several measurements has the same basic circuit with a small ac voltage added to the gate bias V. In this case, as shown in Fig. 2(b), the digital voltmeter is replaced by a lock-in amplifier referenced to the ac component of the gate bias. Capacitance measurements were made using a bias voltage and a 1-MHz Boonton capacitance meter between the gate and the InAs contacts.

IV. RESULTS

A. Interfacial region

One of the experimental procedures used was to determine the conductivity and the Hall coefficient of a layer as it was successively thinned by low-energy (500 eV) argon-ion-beam sputtering from 15 to 0 μm. The results thus obtained are in general agreement with those from epilayers having a variety of thicknesses.[4] The thickness-reduction technique appears to be quite reliable. Using a scanning electron microscope, it is quite obvious (Fig. 3) when the indium arsenide (texture on right side) is etched through to the gallium arsenide (left-hand texture). The initial layer and the sputtering process were found to be sufficiently uniform that the entire area is etched through between two examinations separated by $\frac{1}{2}\ \mu$m. Furthermore, the vertical dimension of the InAs surface texturing is seen to be less than this value.

The measured values of conductivity σ_0 and Hall coefficient R_0 are shown in Fig. 4 as a function of remaining InAs thickness. The measurements were made at 77 K in low

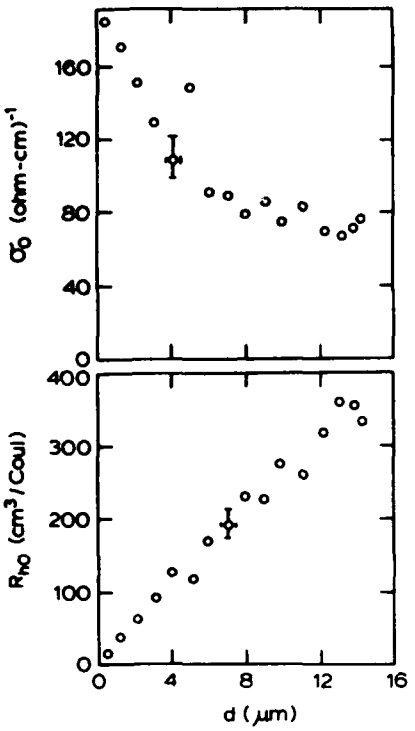

FIG. 4. Measured values of conductivity (a) and Hall coefficient (b) as a function of thickness of the etched InAs. Sample A.

magnetic fields. These results may be interpreted analytically by expressing the electron concentration $n(z)$ and mobility $\mu(z)$ as continuous functions of the direction z normal to the interface. The effective, or measured, value of conductivity is

$$\sigma_0 = \frac{e}{d}\int_0^d n(z)\mu(z)\,dz, \tag{1}$$

and the Hall coefficient in the weak magnetic field approximation is

$$R_0 = \frac{e}{\sigma_0^2 d}\int_0^d n(z)\mu^2(z)\,dz, \tag{2}$$

where d is the thickness of the layer.

One can now take differences between measured values of σ_0 and R_0 to determine n and μ as a function of distance from the substrate:

$$n(z)\mu(z) = \frac{1}{e}\frac{\Delta(\sigma_0 d)}{\Delta d}, \tag{3}$$

$$n(z)\mu^2(z) = \frac{1}{e}\frac{\Delta(R_0\sigma_0^2 d)}{\Delta d}. \tag{4}$$

The values of n and μ extracted in this manner are shown in Fig. 5. Note that this procedure basically consists of measuring the electronic properties of the portion of the epilayer removed by each successive milling step. These are independent of the front-surface parameters, assuming the front surface is identical following each milling increment, even though the milled surface may differ from that as grown.

The behavior of carrier concentration and mobility in Fig. 5 is consistent with the model of Baliga and Ghandi[5] in which the defect formation at the interface leads to a carrier density which decreases exponentially as one moves away from the interface. The corresponding mobility is likely to be dominated by defect scattering, and to first order is inversely proportional to n. The characteristic distance for our InAs samples is seen from Fig. 5 to be about 1 μm, and at 5 μm and above, the layer is essentially bulklike. The bulk values for this epilayer shown are somewhat inferior ($\mu = 3.5\times10^4$ cm^2/V sec; $n = 9\times10^{15}$ cm^{-3}) to those of other samples investigated.

The metallurgical profile of the GaAs/InAs interface, as revealed by Auger measurements on the sample used for the thickness-dependence study, is also shown in Fig. 5. The much sharper transition from gallium to indium dominance (less than 1000 Å) is consistent with what one would expect from vapor-phase growth and the abrupt change in texture mentioned above.

B. Front-surface region

The surface of InAs is known to pin the Fermi level approximately 50 meV above the conduction-band minimum.[6] Thus, n-type material has a heavily accumulated surface under zero bias. Schwartz *et al.*[7] showed that at 77 °K, a high negative gate bias would bring the surface into deep depletion, and they calculated a surface-state density of 2.8×10^{11} cm^{-2} and a fixed oxide charge of $+1.5\times10^{12}$

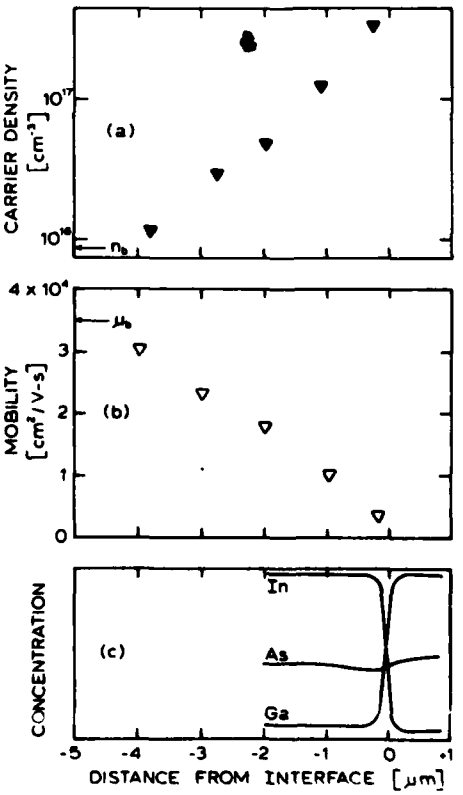

FIG. 5. Profile of carrier density (a), mobility (b), and metallurgical composition (c) in the vicinity of the GaAs/InAs interface. Sample A.

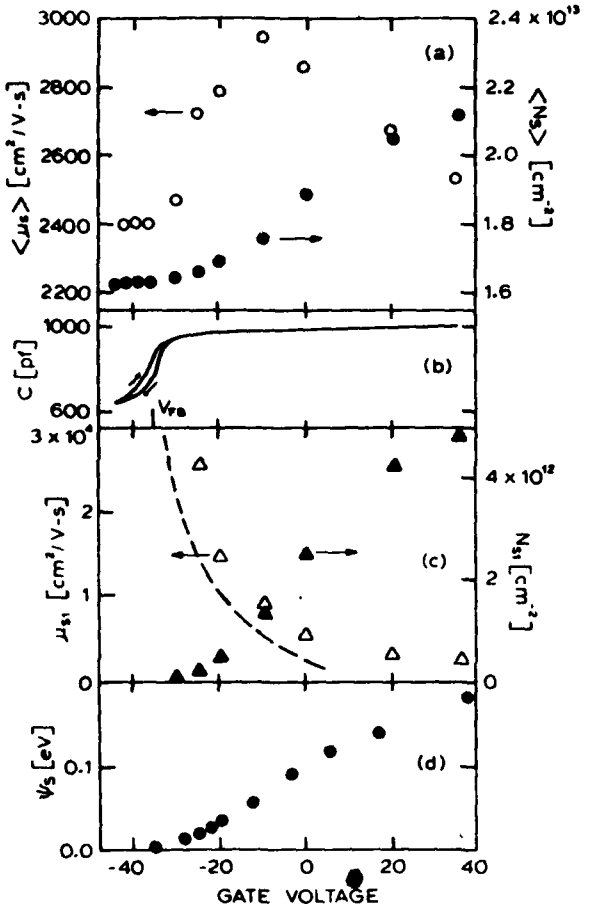

FIG. 6. Gate-voltage dependence of (a) total surface electron density and effective mobility, (b) capacitance at 1 MHz, and (c) front-surface electron density and mobility. Dashed line is calculated mobility. (d) Front-surface potential. Sample B.

cm^{-2}. Further measurements made by Wilmsen *et al.* are in qualitative agreement.[8]

We have measured the gate-voltage dependence of the conductivity and Hall coefficient of MIS InAs structures. The samples used were from a different growth run than those that were milled away in Sec. IV A. They had an average electron concentration of 1.3×10^{15} cm^{-3} and mobility of 1.4×10^{5} cm/V sec at 77 °K prior to the fabrication of the MIS structure.

The values of the total surface electron density $\langle N_s\rangle$ and average surface mobility $\langle \mu_s\rangle$, combining the effects of the two surfaces, are extracted from the 77 °K galvanomagnetic measurements and are shown in Fig. 6(a). The analysis procedure, which has been described previously,[9,10] is to divide the epilayer arbitrarily into a bulklike and a surfacelike region. The flat parts of the Fig. 6(a) curves at large negative bias are interpreted as the depletion region where the front-surface carrier transport is the same as that in the bulk, and the values of $\langle N_s\rangle$ and $\langle \mu_s\rangle$ are to be associated with surface 2 or the interfacial region. This interpretation is supported by the capacitance data shown in Fig. 6(b), where flatband is seen to coincide with the kinks in Fig. 6(a). The value of the surface electron density when the front surface is in depletion is found to be 1.6×10^{13} cm^{-2} and agrees well with the integration of the interfacial density $n(z)$ taken from the sample shown in Fig. 5(a). The surface mobility with the front surface at flatband is 2400 cm^2/V sec and is consistent with the average value of Fig. 5(b), as weighted by the carrier density.

When the gate voltage is varied so that the front surface becomes accumulated, the total surface density increases. This increase, interpreted as the front surface density N_{s1}, is shown in Fig. 6(c). Extraction of the front-surface mobiltiy is somewhat more involved,[10] but leads with semiquantitative reliability to the values of μ_{s1} also shown in Fig. 6(c). The surface mobility becomes quite large as the sample approaches flatband, achieving perhaps the bulk values, but in any case is larger than that reported in inversion layers.[11] For stronger accumulation, the surface mobility falls monotonically. The dashed curve, shown for comparison, is based on a simple calculation based on diffuse surface scattering using a square well surface potential.[12] It is not clear whether the difference in magnitude is due to a form of screening, to a certain amount of specular reflection, or to the magnitude of the surface potential used.

The following qualitative interpretation is proposed for

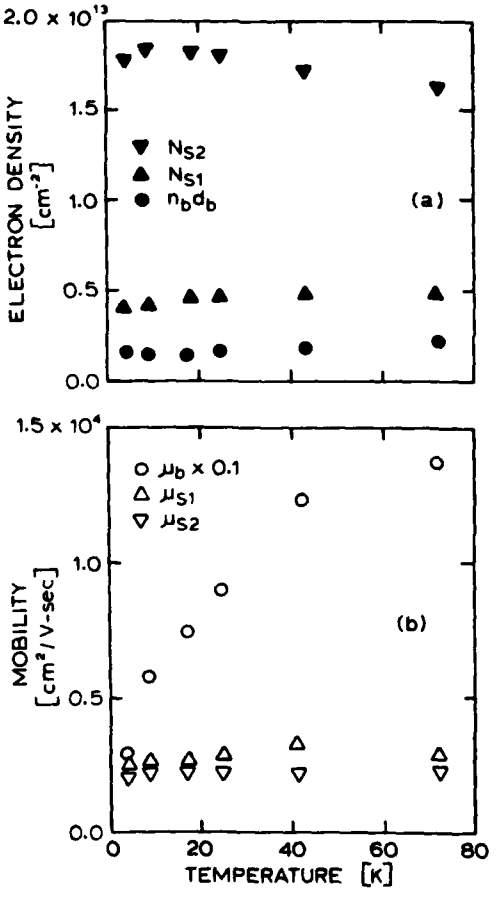

FIG. 7. Temperature dependence of (a) electron density and (b) mobility of each of the three InAs regions. Sample B.

the average surface mobility of Fig. 6(a). In depletion, it is simply that of the interfacial layer. As the front surface begins to be accumulated, however, its higher-mobility electrons are added to the average electron density in increasing numbers, and the average surface mobility goes up. In strong accumulation, though, the front-surface mobility has decreased substantially, probably due to surface scattering, and thus the average surface mobility goes back down.

The values of surface potential shown in Fig. 6(d) are tenuous at best. Since the Fermi level is strongly pinned in InAs, it is difficult to extract the surface potential from either the quasistatic or high-frequency C-V curve. Our simplified approach, therefore, was to take the front-surface density from Fig. 6(c), estimate the density of states and the shape of the well, and calculate how deep the well must be to accommodate all the states. Each step involves a potential error, but the nearly linear dependence of the result is considered correct.

The procedures described above to obtain the 77 °K data were also followed for several other temperatures, and the results allowed extraction of the temperature dependence of the surface parameters. Figure 7(a) show the electron density values for the front surface in strong accumulation ($V_G = 35$ V), for the bulk of the epilayer, and for the back surface. Figure 7(b) shows the corresponding mobility values. Again, the analysis described in Ref. 10 was used. To first order all three density curves are constant with temperature. If the front-surface densities for other gate voltages were plotted, then the N_{s1} curve would simply be decreased to lower magnitudes. In all cases, however, it is substantially lower than the back-surface density. In the case of the mobilities also, both surface values are nearly constant. The effect of lower gate voltages here is to raise the front-surface curve in magnitude. This temperature independence of the surface mobilities contrasts sharply with that of the bulk mobility, which exhibits a strong temperature dependence, attributed to ionized-impurity scattering in this temperature range.[9]

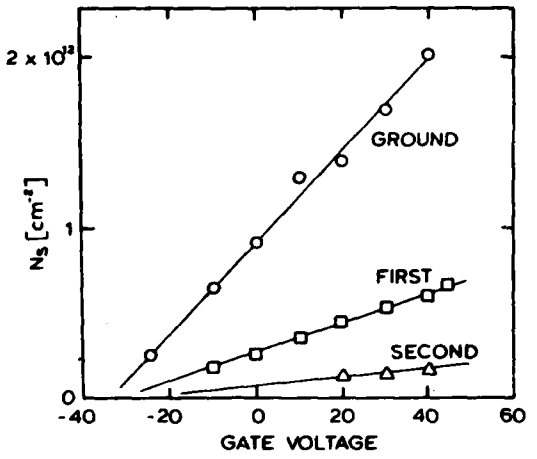

FIG. 9. Subband densities as a function of gate voltage.

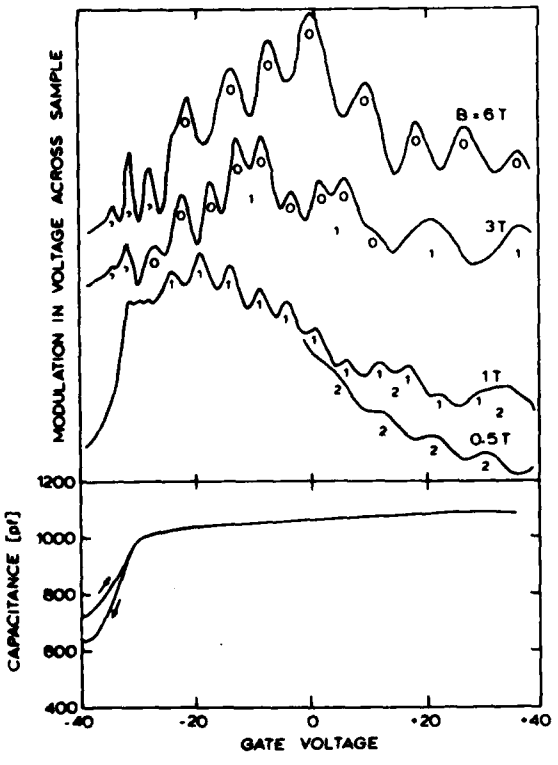

FIG. 8. Shubnikov–de Haas oscillations as a function of gate voltage for four magnetic fields. Oscillations are associated with the ground state (0), first (1), and second (2) excited subbands. Also shown for the flatband reference is the 4 °K capacitance curve. Sample B.

C. Surface quantization

At low temperatures, electrons in the accumulated front surface of an InAs epilayer are found in discrete subbands of the conduction band. Experimentally, this effect leads to Shubnikov–de Haas oscillations in the conductivity as a function of the magnetic field or gate voltage.[13,14] The period of the oscillations is related to the electron density of a subband, and the temperature dependence of the amplitude to the electron effective mass. One can also deduce electron scattering times from the magnetic field dependence of the oscillation amplitudes.[15]

The Shubnikov–de Haas oscillations can be seen in the dc measurements using the circuit shown in Fig. 2(a), but the amplitudes are not large enough for accurate analysis. A differential technique was used, therefore, in which the gate voltage was modulated slightly, and the resulting modulation in voltage across the sample detected with a lock-in amplifier. Two InAs samples were studied extensively, one of them being the same as used in Sec. IV B.

The output of the lock-in amplifier yields curves such as those depicted in Fig. 8. In general, the ground-state subband is dominant at gate voltages near flatband and at high magnetic fields. It leads to the peaks labeled 0, while the first and second excited-state subbands produce the peaks labeled 1 and 2, respectively. Often there is a mixing of oscillations from more than one subband, as shown in Fig. 8. At gate voltages below flatband, the oscillations disappear. For comparison, the capacitance curve also is shown, demonstrating that the onset of oscillations does indeed occur at flatband.

As the temperature is increased these oscillations vanish.

For analysis, the conductivity oscillations are generally plotted against the magnetic field, and the period in inverse field is calculated. The density of the subband N_{si} (i) can now be extracted from

$$N_{si}^{(i)} = \frac{e}{\pi\hbar\Delta(1/B)} = \frac{4.84\times10^{10}}{\Delta(1/B)}\,\mathrm{cm}^{-2}, \qquad (5)$$

where i is 0, 1, or 2, and the field B is in teslas. These surface electron densities are shown in Fig. 9, and they show an increase in density with gate voltage, as expected. Each higher subband appears at successively higher gate voltages and suggests that still higher energy subbands might appear if the experiment were pursued to higher voltages and deeper wells.

The temperature dependence of ground-state oscillations at three gate voltages are shown in Fig. 10. From this data, it is possible to calculate the effective mass for carriers in the surface potential well using the theoretical dependence[16]

$$\text{Amplitude} \sim \frac{2\pi^2kT/\hbar\omega_c}{\sinh(2\pi^2kT/\hbar\omega_c)}, \qquad (6)$$

where $\omega_c = eB/m^*$. The solid curves in Fig. 10, for example, were calculated from Eq. (6) with $m^*/m_e = 0.02$, 0.04, and 0.06.

In practice, some corrections must be made to the data because there is a temperature dependence of the scattering times[17] and because the accumulation layer is in electrical contact with the remainder of the epilayer. We assume, however, that since the front-surface mobility shown in Fig. 7 is essentially temperature independent, the lifetimes are very nearly constant.

The weighting of quantum oscillations by the rest of the epilayer was determined using the analysis of Sec. IV B as elaborated in Ref. 10. The effect is found to be a function of gate voltage, magnetic field, and temperature. For a given oscillation peak at constant magnetic field, however, only the temperature dependence of the bulk mobility shown in Fig. 7 is a factor. For the ground-state oscillation at 6 T, the bulk-layer shunting resulted in a maximum correction to the

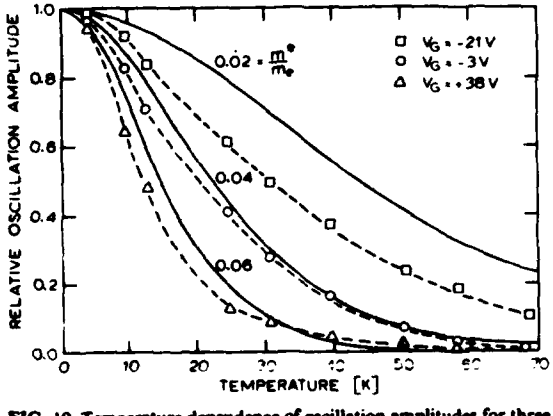

FIG. 10. Temperature dependence of oscillation amplitudes for three gate voltages. Sample B. Solid lines are theoretical curves for three effective masses.

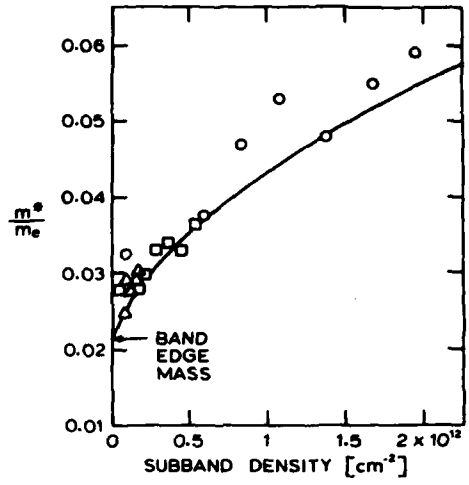

FIG. 11. Effective masses of the ground state (circle), first excited (square), and second excited (triangle) subbands as functions of their respective densities. Solid line is calculation.

calculated effective masses of 20%. The resulting values are plotted in Fig. 11.

The effective masses exhibit a monotonic increase with density somewhat more dramatic than that observed in silicon.[19] Such behavior can be explained with the Kane model for nonparabolic bands,[19] and the resulting alteration of the dispersion relation produced by the surface potential.[20] The solid curve in Fig. 11 was calculated from the dispersion relation in Ref. 20 using an exponential approximation[21] to the surface potential well. The experimental values are in reasonable agreement.

Also shown in Fig. 11 are effective masses calculated for the first and second excited subbands using data taken at 2.0 and 0.5 T, respectively. At these lower fields, the effect of the bulk-layer shunting is greater, and the corrections can increase the effective masses by as much as 50%. Although these values are considered less reliable, they also exhibit increases with density of carriers in the respective subbands. The increase of excited-subband effective mass is predicted[20] to be greater than that for the ground state, but we do not have sufficient sensitivity to make such a contrast.

V. CONCLUSIONS

Careful attention must be given to the effects of both surfaces of InAs epilayers in the evaluation of electrical and galvanomagnetic measurements. Electron mobilities can easily be over an order of magnitude less than those in the bulk. Furthermore, since the interfacial region between an epilayer and its GaAs substrate shows electronic inhomogeneities that extend for a few microns, it may not be possible to utilize extremely thin layers of this type. In fact, if there is a lattice mismatch in epitaxial growth, the result is a defect-dominated layer whose thickness is a function of the mismatch and the compositional grading.

The zero-bias front-surface mobility of InAs is also substantially reduced from that of the bulk, and it seems to be quite temperature independent at temperatures below that

of liquid nitrogen. It does change considerably, however, when the surface potential is varied, extrapolating to near bulk values at flatband. The effective mass of the front-surface electrons is also subject to large changes as the surface potential is varied; it may increase as much as a factor of 3 above its band-edge value.

ACKNOWLEDGMENTS

We are grateful to Charles Parkerson for growing the InAs epilayers, to John Wager for the Auger measurements, to Curtis Haynes for the SEM work, and to Robert Leisure for use of the superconducting magnet. We appreciate several useful discussions with David Ferry, and we particularly acknowledge the support of the Office of Naval Research under Contract N00014-76-C-0976.

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APPENDIX G

ION BEAM SPUTTERED AlO_xN_y ENCAPSULATING FILMS

Hulya Birey,[a] Sung-Jae Pak,[b] and J. R. Sites

Department of Physics

and

J. F. Wager

Department of Electrical Engineering

Colorado State University, Fort Collins, Colorado, 80523, USA

ABSTRACT

The encapsulating properties of 800-1500 Å aluminum oxynitride (AlO_xN_y) films, deposited on GaAs by low energy ion beam sputtering, were studied over a range of y from 0.1 to 0.8. Particular attention was given to chemical and sputter cleaning procedures. The structures were characterized by optical microscopy, electrical conductivity, Auger profiling, and ellipsometry. The better films were found to withstand annealing to above 900°C with minimal physical deterioration. The films with a higher proportion of oxygen allowed some oxygen diffusion; those made with inferior cleaning procedures an out-diffusion of arsenic.

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a) Permanent Address: Physics Department, Istanbul Univ., Istanbul, Turkey

b) Permanent Address: Science Education Department, Seoul National University, Seoul, Korea

APPENDIX H
SUNG-JAE PAK

The specific objectives of this study are investigations of (1) the pumping characteristics, such as foreline and hydrogen vapor pressure and cryopump loading, and (2) of the dependence of the argon ion beam current on various independent variables, such as argon pressure, discharge voltage, and cathode current.

II. VACUUM PUMPING CHARACTERISTICS

1. Vacuum Pumping Station and Deposition System

The vacuum pumping system (CHA Model #SEC-600-RAP) is designed for high pumping speed, low ultimate pressure, and a clean high vacuum system.[10] All stainless steel construction is used to minimize impurities from the system.

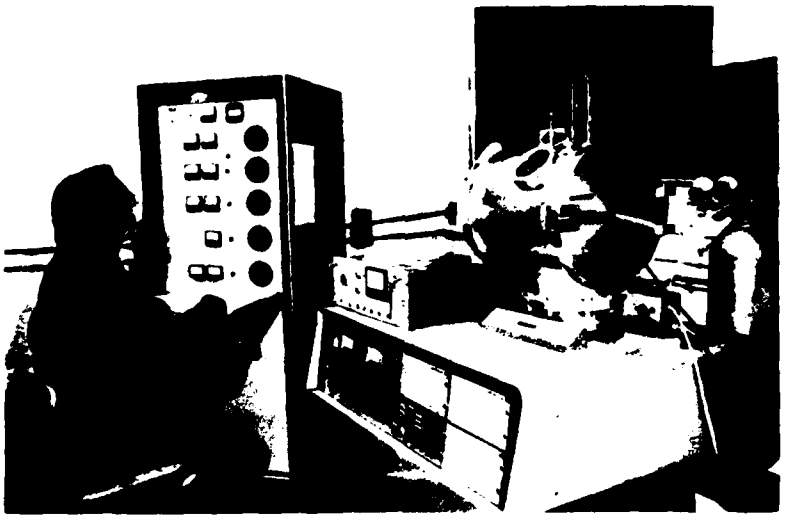

Figure 1. Cryopumped ion beam sputtering system operated by the author

APPENDIX I

ABSTRACT OF DISSERTATION

DIELECTRIC-SEMICONDUCTOR INTERFACES OF

GALLIUM ARSENIDE AND INDIUM PHOSPHIDE

This thesis reports an experimental investigation of the properties of insulator-semiconductor structures formed using the semiconductors InP and GaAs in conjunction with a number of dielectrics. The insulators studied on GaAs were the native oxide formed by anodization, sputtered-silicon nitride, and pyrolytically-deposited silicon nitride. The investigation of InP was limited to the study of pyrolytically deposited silicon dioxide layers. Capacitance-voltage (C-V) measurements over a wide frequency range and surface photovoltage measurements on metal-insulator-semiconductor (MIS) diodes formed from these structures were used to determine the bulk doping, surface potential variation, and interface state density of the semiconductor.

The data on GaAs indicate that on n-type substrates the Fermi level at the surface is pinned at a point 0.8 - 0.9 eV below the conduction band minimum (CBM). Surface potential variations of only $\sim$ 0.4 V are possible around this position. Results on p-type material were in agreement except that the zero bias position of the Fermi level at the surface was 0.7 - 0.8 below the CBM. Accumulations of neither electrons nor holes were observed on the GaAs samples for surface electric field magnitudes to to 16^6 V/cm. A minimum surface state density of 2×10^{12} cm^{-2} eV^{-1} was calculated near the zero bias position with values greater than 10^{14} cm^{-2} eV^{-1} as the band edges were approached.

Data on the n-type InP samples indicate that the surface is near flatband with zero applied gate bias. With applied electric fields of

APPENDIX I

$\pm 10^6$ V/cm the surface could be modulated from accumulation into or nearly into inversion. The surface state density rose from 6×10^{11} cm^{-2} eV^{-1} at a point 0.6 eV below the CBM to 2×10^{12} cm^{-2} eV^{-1} at flatband. Data on the p-type samples indicated that the surface is near inversion with zero gate bias. The surface could be fully inverted with positive gate bias; however, the surface did not reach flatband with negative gate bias. This apparent discrepancy between the data on the n- and p-type material was not fully resolved.

LARRY G. MEINERS
Physics Department
Colorado State University
Fort Collins, CO 80523
Spring, 1979

APPENDIX J

Radiative transitions induced in gallium arsenide by modest heat treatment

Hülya Birey[a] and James Sites
Physics Department, Colorado State University, Fort Collins, Colorado 80523

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Photoluminescence spectra from three species of *n*-GaAs, lightly Si doped, heavily Si doped, and lightly Te doped, show the onset of additional radiative transitions upon modest annealing in the 550–700 °C range. Etch-back procedures reveal that the new structure is all surface related. It is attributed to the creation of arsenic vacancies at the surface which allow electrical activation of silicon donors, enhance the probability of silicon site exchange, and lead to complex formation involving both donor and acceptor levels.

PACS numbers: 78.55.Ds

I. INTRODUCTION

Photoluminescence (PL) has been extensively used to characterize many of the impurity and defect energy levels in gallium arsenide.[1–9] Some of these levels have been unambiguously identified, while others have been the subject of speculation and controversy. In particular, there are many situations in which the transition appears to involve a complex of more than one impurity or vacancy. These transitions are often rather broad, sample dependent, and have a peak wavelength that depends on excitation intensity.

The purpose of this paper is to study the effects of modest heating of bulk gallium arsenide, and to attempt to identify the fundamental changes in the material insofar as they can be deduced from the PL spectra. In this study, we have chosen three different types of *n*-doped GaAs, and have carefully measured the effects of controlled annealing on their PL emissions. We have then integrated our observations with those of other authors to form what we believe is a consistant model of the thermal effects.

II. EXPERIMENTAL

The GaAs samples studied were ⟨100⟩ orientation single-crystal wafers. As far as we could establish, they were all grown in silica as opposed to graphite crucibles, and thus unintentional impurities are likely to be silicon and unlikely to be carbon.

The PL measurements were made with the relatively straightforward apparatus shown in Fig. 1. Samples were mounted on the cold finger of a cryogenic Dewar that could be operated with either liquid helium or liquid nitrogen. Estimated sample temperatures for these two modes of operation were 12 and 90 °K, respectively. The warm up rate after liquid helium boiled away from the chamber shown was about 15 °K/h, allowing sufficient time to make temperature-dependent measurements over the intermediate range. Further heating above 90 °K was also possible. The actual Dewar used had four light-entry windows and was equipped to measure four samples each cool down.

The PL excitation source was a 50-mW 6328-Å He-Ne gas laser. The beam was attenuated by a variable-density filter, modulated by a 40-Hz mechanical chopper and focused to approximately 1 mm^2 at the sample. The emitted radiation was focused onto the entrance slit of a 0.5-m grating spectrometer, taking care that the reflected laser light missed the slit. A silicon *p-i-n* detector was mounted directly over the exit slit of the spectrometer. Its sensitivity covered the 8000–10 500-Å range of interest, although some correction must be made for magnitudes of spectral lines above 10 000 Å. The current output from the detector was amplified and converted to a voltage which became the input signal of a lock-in amplifier referenced to the chopper driver. The lock-in output was connected to an *x-y* recorder for preserving the spectra.

Thermal annealing of the GaAs samples was done in a temperature-controlled quartz furnace. They were exposed to a continuous flow of hydrogen gas. Annealing temperatures were concentrated in the 550–700 °C range and times were varied from 10 to 150 min. Samples were kept in the flowing H_2 atmosphere until they cooled to ambient temperature. Etching procedures to establish the depth of the thermally induced transitions were done using a sulfuric acid solution. A part of the sample was protected during the etch, and the depth of the resulting step was measured with a scanning electron microscope.

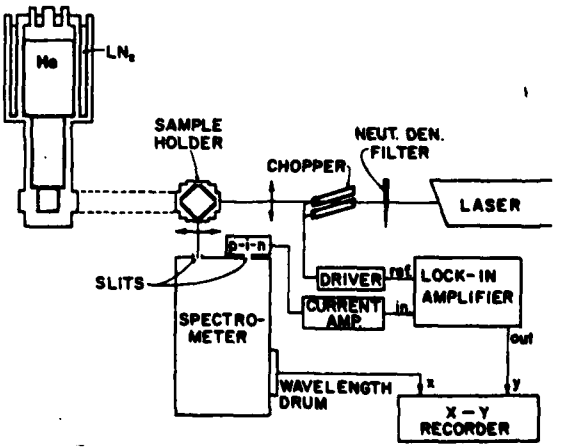

FIG. 1. Schematic of photoluminescence apparatus.

[a]Permanent Address: Physics Department, Istanbul University, Istanbul, Turkey.

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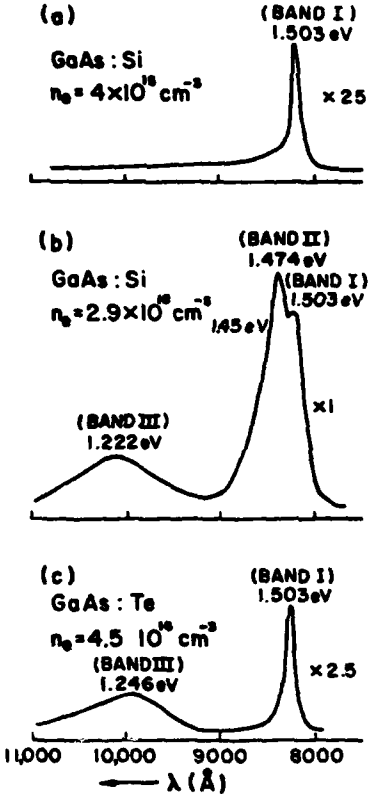

FIG. 2. PL spectra of three types of GaAs examined at 90 °K.

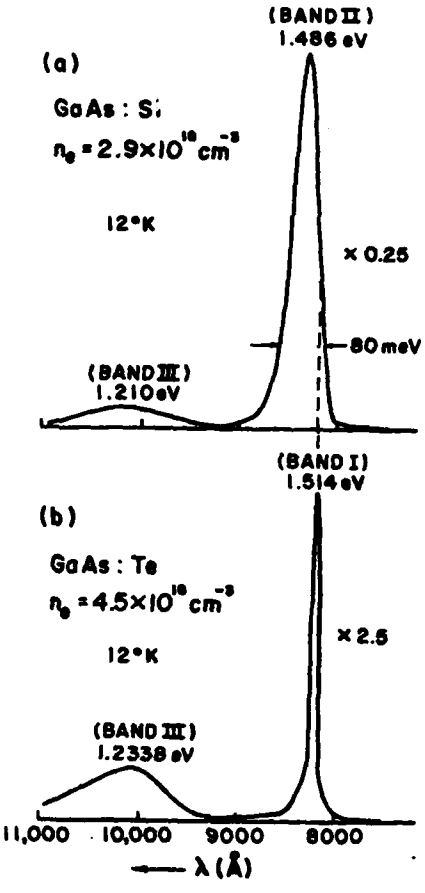

FIG. 3. PL spectra at 12 °K.

III. RESULTS AND DISCUSSION

A. As-grown material

The PL spectra from annealed samples of the three types of GaAs studied are shown in Fig. 2 at a temperature of 90 °K and again at 12 °K in Fig. 3. There are three classes of emission lines observable in PL spectra of corresponding samples. Both the lightly doped silicon ($n = 4\times10^{15}$ cm^{-3}) and the lightly doped tellurium (4.5×10^{16} cm^{-3}) samples show a narrow peak at 1.503 eV for 90 °K and 1.514 eV at 12 °K, in each case about 7 meV lower than the band gap for those temperatures.[10] This energy corresponds closely to that of a simple hydrogenic donor impurity[11] and is assumed to result from silicon on a gallium site (Si_{Ga}) in the first case and tellurium on an arsenic site (Te_{As}) in the second. We will refer to this donor-valence band (D-B) transition as Band I. This transition as well as the other assignments we make to the as-grown material are shown in Fig. 4.

In the heavily doped silicon ($n = 3\times10^{18}$ cm^{-3}) material, there is a second peak labeled Band II at 1.474 eV for 90 °K which moves progressively to 1.486 eV at 12 °K [see Fig. 5(a)]. Band I is also present in these samples at the higher temperatures, but becomes unresolvable at about 35 °K [Fig. 5(b)]. Both of these peaks are somewhat wider in the heavily doped material than Band I is in the lightly doped samples. We attribute Band II to a donor-acceptor (Si_{Ga}-Si_{As}) transition (see Fig. 4) since silicon is known to be an amphoteric donor in GaAs, and is found on both gallium and arsenic sites in heavily doped material. The energy of Band II differs from Band I by 28 meV, which is consistant with the energy of a hydrogenic acceptor impurity. The increasing dominance of the donor-acceptor transition is interpreted as the decrease in acceptor ionization with lower temperature. Further evidence that Band II involves a donor-acceptor pair comes from shift of the line to higher energies with increased excitation intensity (1.2 meV/decade in our case) and narrowing of the line (1 meV/decade). Following the argument of Leite and DiGiovanni,[12] there is a coulombic term in a donor-acceptor transition with a spatial energy dependence, and higher intensity excitation light increases

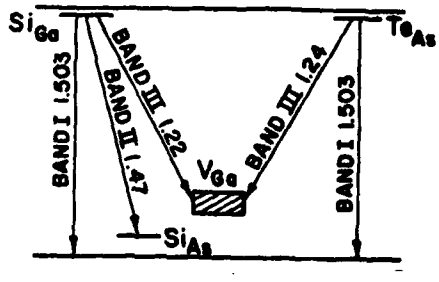

FIG. 4. Suggested energy diagram for as-grown GaAs : Si, Te.

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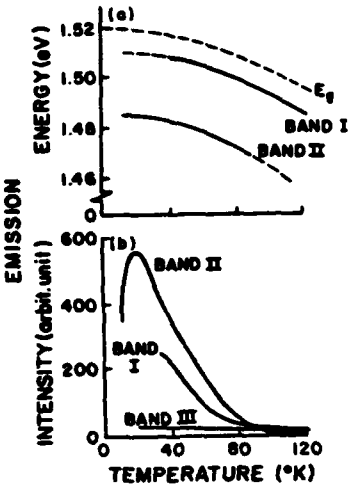

FIG. 5. Temperature dependence of (a) PL peak energy and (b) PL intensity for heavily doped GaAs : Si.

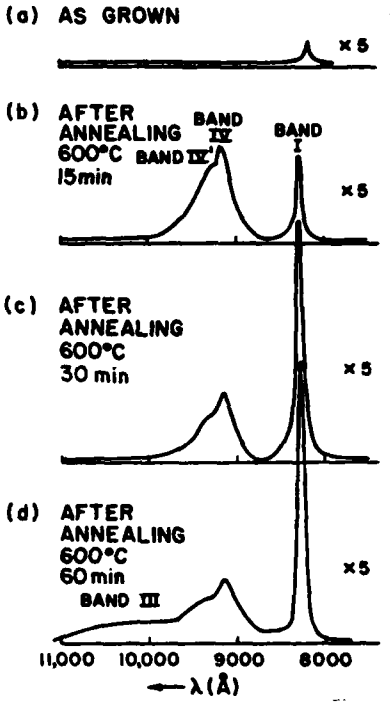

FIG. 6. Evolution of PL spectrum with annealing time for $n = 4 \times 10^{15}$ cm^{-3} GaAs : Si.

the probability of transitions from donors to nearby acceptors.

The third major feature in the unannealed samples is the broad peak near 1.2 eV appearing in both the tellurium and the heavily doped silicon samples. This structure, labeled Band III, is generally attributed to a complex consisting of a donor impurity and a gallium vacancy acting as singly charged acceptor.[13] The observed transitions (see Fig. 4) would, therefore, be (Si_{Ga}-V_{Ga}) and (Te_{As}-V_{Ga}). In the tellurium case, this transition is observed, in agreement with Williams,[13] to occur at a slightly higher energy, presumably because the Group-VI donor Te can be adjacent to the vacancy, while the Group-IV donor silicon, must be at least a second neighbor site away. The lightly doped Si samples do not show Band III, due, one assumes, to a lack of gallium vacancies. In the other as-grown samples, the intensity of Band III is essentially independent of the measuring temperatures.

B. Heat treated material

The PL technique was next used to examine changes in the radiative transitions in GaAs due to heat treatment. All of the peaks observed in the PL spectra for the various samples both before and after annealing are tabulated in Table I.

TABLE I. Summary of PL energies.

Sample properties	Annealing temp (°C)	Annealing time (min)	Temp during experiment (°K)	Emission peaks (eV) Band I (D-B)	Band II (D-A)	Band III complex	Band IV complex	Band IV' p. replica	Band V (D-A)	Band VI complex
GaAs : Si		none	90	1.503						
$n = 4\times10^{15}$ cm^{-3}	600	15	90	1.501			1.36	1.329		
⟨100⟩	600	30	90	1.499			1.36	1.329		
	600	60	90	1.501	1.475	1.22	1.36	1.329		
GaAs : Si		none	90	1.503	1.476	1.22				
$n = 3\times10^{16}$ cm^{-3}		none	12		(1.486)	(1.21)				
⟨100⟩	600	15	90	1.495	1.467	1.26			1.44	
	600	60	90	1.495	1.467	1.27	1.36		1.44	
	600	60	12		(1.482)	(1.250)	(1.37)		(1.44)	
	700	15	90			1.26	1.36		1.44	
GaAs : Te		none	90	1.503		1.29				
$n = 4.5\times10^{16}$ cm^{-3}		none	12	(1.512)		(1.23)				
⟨100⟩	600	15	90	1.503		unresolved	1.352			1.31
	600	30	90	1.503	1.47	unresolved	1.352			1.31
	600	30	12	(1.512)	(1.486)	unresolved	(1.365)			(1.32)
	600	60	90	1.503	1.474	unresolved	1.352			1.31
	700	15	90	1.50	1.474	unresolved	1.352			1.31

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The evolution of the 90 °K PL spectrum from lightly doped GaAs : Si for successively longer annealing times is shown in Fig. 6. The first feature of interest is the growth in intensity of Band I, the donor-to-band transition. Similar behavior is observed in a slightly more heavily doped sample from a different manufacturer. This increase in intensity involves only material in the first few microns from the surface, as determined from etch-back procedures. Since the lightly doped material is known to be partially compensated, it is possible that the additional donors are being transfered from acceptor sites, a situation presumably enhanced in the surface region by a higher incidence of vacancies. An alternative explanation is that the additional silicon could diffuse into the GaAs from external sources, such as the quartz annealing tube.

The second major feature of the lightly doped GaAs : Si is the almost immediate appearance, and then gradual decrease, of a peak at 1.36 eV (Band IV') and a smaller companion at 1.33 eV (Band IV). This structure has been observed by many authors, and has been explained in different

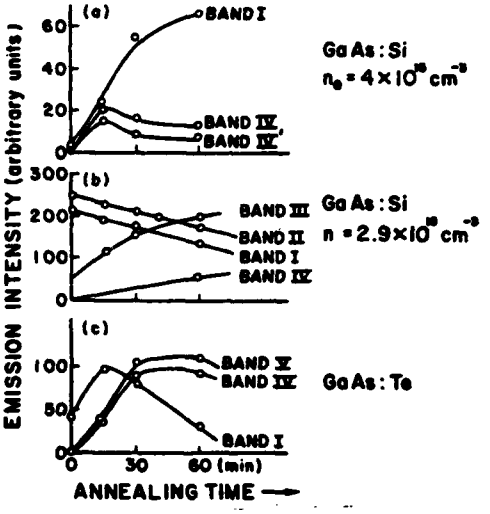

FIG. 8. PL intensities versus annealing time for (a) n^--GaAs : Si (b) n^+-GaAs : Si and (c) n-GaAs : Te.

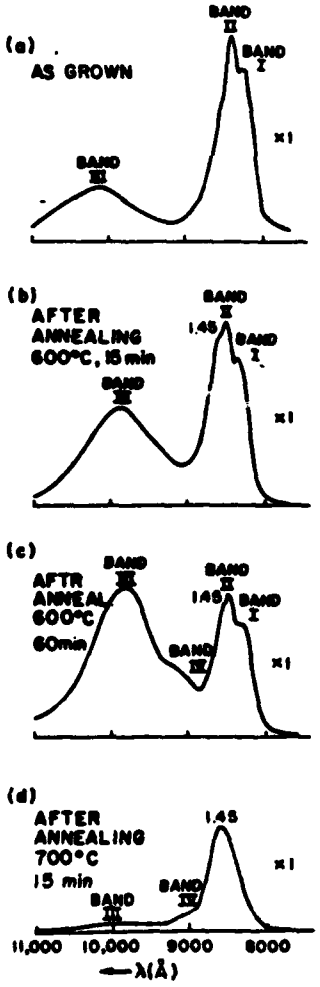

FIG. 7. Evolution of PL spectrum for $n = 3\times10^{18}$ GaAs : Si.

ways.[3,7,9,14] The major peak is interpreted by us as an arsenic vacancy-silicon complex (V_{As}-Si_{As}), and the smaller as the first phonon replica corresponding to the 36-meV LO phonon in GaAs. Since this peak, in our viewpoint, involves Si on As sites, it is logical that it would diminish as the donor peak grows. A very similar looking peak, incidentally, occurs in GaAs with carbon impurities at 1.41 eV and is accompanied by phonon replicas at 1.38 eV and 1.34 eV.[5,15] We assume that the 1.41-eV transition is (V_{As}-C_{As}). One report, in fact, finds the 1.36-eV structure when GaAs is annealed in contact with a silicon compound, and the 1.41-eV structure when it is adjacent to graphite.[16] It would seem reasonable to assume that other acceptors in GaAs will form similar complexes and may, in fact, be indistinguishable from (V_{As}-Si_{As}).

The final feature to appear upon modest annealing (Fig. 6) for longer times is Band III, not previously seen in the lightly doped GaAs : Si samples. The explanation here is that eventually enough arsenic vacancies form near the surface that it becomes statistically favorable for the reaction $V_{As} + Si_{Ga} \leftrightarrow V_{Ga} + Si_{As}$ to proceed to the right, leading to a finite concentration of gallium vacancies. At the same time, we see a very small feature at 1.47 eV, the position of the peak previously attributed to a (Si_{Ga}-Si_{As}) donor-acceptor transition. Both these peaks are eliminated by etching a few microns from the surface.

The time evolution of the 90 °K PL spectrum from a heavily doped GaAs : Si specimen is shown in Fig. 7. No significant differences in the evolution were observed at 12 °K. In Figs. 8(a) and 8(b), the evolution of the major peaks in the lightly and heavily doped samples are compared, and one observes that the changes in the spectrum from the heavily doped material are much less dramatic. In Fig. 8(b), we do see a roughly parallel increase in Bands III and IV (1.2 and 1.36 eV) and corresponding decrease in Bands I and II for the single impurity transitions. Again we

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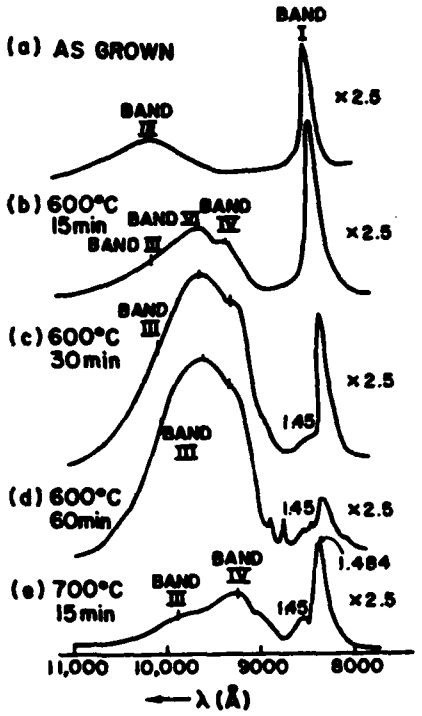

FIG. 9. Evolution of PL spectrum for $n = 4.5 \times 10^{16}$ GaAs : Te.

attribute the basic physical change in the GaAs to the in-diffusion of arsenic vacancies leading to complex formation and the subsequent creation of gallium vacancies through silicon site exchange. As before, the additional structure can be eliminated by etch-back techniques.

Of additional interest is the heavily doped silicon material in the development of a peak at 1.44 eV (Band V). This peak is clearly distinguishable from the 1.47-eV peak and in fact is just resolvable in the as-grown material (Fig. 7). It is presumably the peak first discussed by Queisser[17] in even more heavily doped GaAs : Si. Following the suggestion of Kressel, *et al.*,[3] we think it reasonable to attribute Band V to a donor-acceptor complex of silicon on two adjacent sites, distinguishable from the standard Si_{Ga}-Si_{As} transition at 1.47 eV. We observe that the next larger Si_{Ga}-Si_{As} distance is nearly twice $(11/3)^{1/2}$ the near neighbor distance. After higher temperature annealing (Fig. 7), there is a general decrease in the intensity of Band III and a further shift from Band II (1.47 eV) to Band V (1.44 eV), explained as a tendency for silicon impurities to cluster on neighboring sites.

The GaAs : Te PL evolution is given in Fig. 9. There is a small initial increase in Band I and the immediate appearance of Band IV (1.36 eV). We attribute these features to silicon impurities with identical effects as in the lightly Si-doped samples, silicon being present likely because of the silica container for the original crystal growth. The most prominent feature in Fig. 9, however, is the appearance of a new peak at 1.31 eV, labeled Band VI. This peak is definitely not a phonon replica of the 1.36-eV peak. It is too large and occurs at the wrong energy; it would, however, mask any

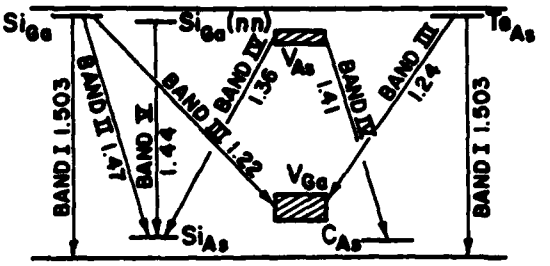

FIG. 10. Suggested energy diagram for common transitions in heat treated GaAs. 1.31-eV transition for Te doping not shown (see text).

phonon replicas from Band IV. We believe that this new band probably results from a transition from the tellurium donor to a nearby arsenic vacancy acting as an acceptor (Te_{As}-V_{As}). It has a width and shape (no phonon replica) quite reminiscent of acceptor bands due to gallium vacancies, but its energy is much larger. This peak, which is also seen in more heavily doped GaAs : Te from two different manufacturers, is presumably related to the primary dopant, and it seems very unlikely that tellurium would act as an acceptor. An arsenic vacancy, on the other hand, holds the possibility of pairing the extra electron almost as well by being an acceptor as by being a donor. An alternative explanation, however, is the existence of the other unknown impurity, creating a new deeper acceptor level in the crystal.

IV. CONCLUSIONS

Based on fairly careful photoluminescence measurements of moderate temperature-annealed gallium arsenide, we have constructed (Fig. 10) a tentative energy level diagram for the common impurities, silicon and telurium, and their complexes with vacancies. With the exception of the 1.31-eV line in GaAs : Te, all the spectral features described above are represented.

The basic trigger, in our opinion, for the transitions which we see develop during modest anneal cycles, is the formation of arsenic vacancies at the GaAs surface. These include (1) a growth of the 1.503-eV donor-band transition in lightly doped GaAs : Si, (2) the appearance of the 1.36-eV arsenic vacancy-acceptor complex transition in all samples, (3) the appearance of the 1.44-eV complex line in heavily doped GaAs : Si, and (4) the appearance of a broad 1.31-eV peak in GaAs : Te. We appreciate that this picture is subject to some discussion, but we feel that it is supported by the bulk of the evidence currently available.

ACKNOWLEDGMENTS

We are grateful to Joe Bowden for the construction of the original photoluminescence apparatus and to Harry Wieder and Larry Lum for many provocative and useful discussions. We particularly ackowledge the support of the U.S. Office of Naval Research through Contract N00014-76-C-0976, and the Scientific and Technical Research Council of Turkey and Istanbul University.

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APPENDIX K

THICKNESS AND REFRACTIVE INDEX OF THIN TRANSPARENT FILMS BY SPECTROPHOTOMETRIC TRANSMISSIVITY

by Hülya Birey*

Physics Department
Colorado State University
Fort Collins, CO 80523 U.S.A.

Interference effects in the transmission spectrum of transparent films are used to simultaneously extract the index of refraction and the thickness. Excellent agreement with other techniques is found for AlN films on glass substrates.

*Permanent Address: Istanbul University, Faculty of Science
Physics Department, Istanbul, TURKEY

APPENDIX L

Photoluminescence of gallium arsenide encapsulated with aluminum nitride and silicon nitride

Hulya Birey,[a] Sung-Jae Pak,[b] and J. R. Sites
Department of Physics, Colorado State University, Fort Collins, Colorado 80523

(Received 29 June 1979; accepted for publication 15 August 1979)

Aluminum nitride and silicon nitride films were deposited on lightly doped *n*-type GaAs:Si by low-energy ion beam sputtering. Mechanically, the films were stable at annealing temperatures above 900°C. In contrast to bare GaAs and previously reported encapsulation with Si_3N_4, where the 1.36-eV line appears at relatively low annealing temperatures, there was no change in the photoluminescence spectrum until the samples were annealed at 800°C in the case of aluminum nitride and 900°C for silicon nitride.

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[a]Permanent address: Physics Department, Istanbul University, Istanbul, Turkey.
[b]Permanent address: Science Education Department, Seoul National University, Seoul, Korea.

Gallium arsenide that is doped by implantation must be annealed to relieve structural damage. One technique for preventing the loss of arsenic during the annealing process is

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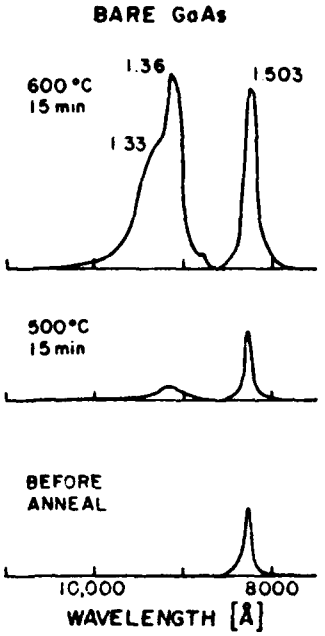

FIG. 1. Appearance of 1.36-eV and growth of 1.503-eV PL lines. Data taken at 90 K before and after bare GaAs : Si ($n = 4 \times 10^{15}$ cm $^{-3}$) is annealed at 500 and 600 °C. Same scale for each spectrum.

to encapsulate the GaAs surface with a deposited dielectric layer that can withstand high temperatures. In this letter, we report the results of encapsulation with silicon nitride and aluminum nitride films as revealed primarily through photoluminescence (PL) studies.

Characteristic of what happens at a GaAs surface that is not encapsulated is shown in Fig. 1. The *n*-type GaAs used had only a very light doping of silicon (4×10^{15} cm^{-3}) so that there would be a high degree of sensitivity to any changes in the PL spectrum. As reported previously,[1] the initial spectrum has only a single near band-gap peak at 1.503 eV and is not sensitive to the measurement temperature below 100 K. Upon annealing, however, a distinctive feature appears at 1.36 eV. It is attributed[2] to an arsenic-vacancy–silicon-acceptor complex, although other authors[3,4] disagree. The 1.33-eV lower energy shoulder, in any case, is the LO phonon replica. In our work, the appearance of the 1.36-eV line was first noticeable at 500 °C annealing and became dominant at 600 °C. Additionally, we observed considerable growth of the 1.503-eV line at the same temperature, and visual observation showed that the polished surfaces had become significantly duller.

Considerable effort has been given to developing techniques for depositing silicon nitride,[5-9] and to a lesser extent, aluminum nitride,[10,11] for encapsulation purposes. The technique we employ is low-energy ion beam sputtering[12] using a neutralized beam, primarily nitrogen, impinging on a pure aluminum or silicon target. Deposition takes place simultaneously on GaAs and Corning 7059 glass substrates which are rotated during the process. Generally, both target and substrate are lightly sputter etched *in situ* before deposition; the substrates remain near room temperature throughout the process. The sputter beam energy used most successfully was 800 eV. The AlN depositions used a pure nitogen beam, while the Si_3N_4 seemed to work best with a 15% admixture of argon. Typical deposition time was 20 min resulting in films of the order of 800 Å thick. Both the AlN and Si_3N_4 films on glass were quite transparent (~90% transmission) from 0.3 to 3 μm. Auger analysis showed that the primary impurity was oxygen, having a concentration near 5% in both the AlN and Si_3N_4 films. Other impurities were considerably lower and probably unimportant. Neither the predeposition sputter etch nor the deposition itself leads to any significant changes in the PL spectrum.

The development of the PL spectrum for the AlN encapsulated GaAs, at successively higher annealing tempera-

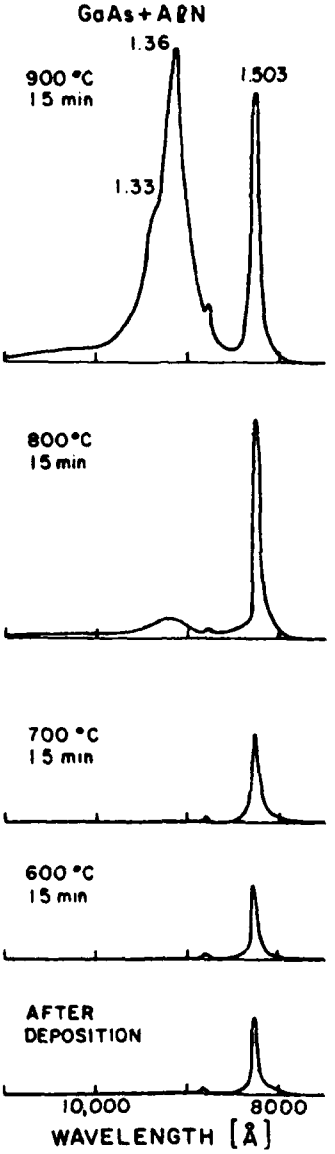

FIG. 2. Onset of the PL features when same GaAs is encapsulated with AlN using ion beam sputtering and then annealed. Same scale as Fig. 1.

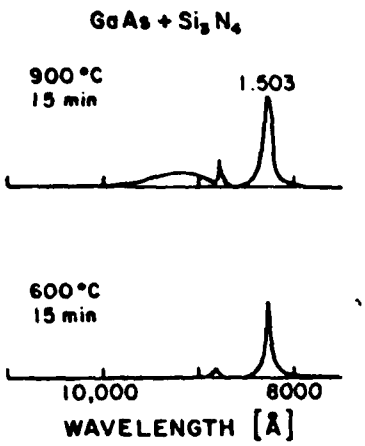

FIG. 3. Higher temperature onset of PL change when GaAs is encapsulated with Si_3N_4 prior to annealing. Same scale as Fig. 1.

tures, is shown in Fig. 2. The same low carrier concentration GaAs is used, and the scale is the same as in Fig. 1. Basically, the same pattern is seen except that 300 additional degrees of annealing temperature are gained before changes begin. In addition to the growth of the 1.503-eV line and the onset of the 1.36-eV peak, we did observe a small feature at 1.40 eV, also seen in other work.[2] Even at 900 °C, however, there is no observable visual deterioration (under 400× magnification), no shift in refractive index, no decrease in transparency, and no change in Auger profile. Other AlN samples studied show basically the same PL development, except in some cases the growth of the 1.503-eV line precedes the onset of that at 1.36 eV.

In the case of Si_3N_4 encapsulation, the PL spectrum remains unchanged until still higher temperatures. As with the AlN films, there are no other signs of deterioration of the Si_3N_4 layers. Figure 3 illustrates the PL onset, omitting the uninteresting intermediate temperatures. This higher temperature onset shows an improvement over our earlier Si_3N_4 results[9] where in more heavily doped material we saw the onset of the 1.36-eV line at 600 °C. The difference, we believe, is due to an increase in our sputter beam energy from 500 to 800 eV and an increase in the nitrogen fraction of the beam.

In summary, we have succeeded in depositing dielectric layers of aluminum nitride and silicon nitride that appear to be useful for the encapsulation of gallium arsenide. We feel that good results are attributed to general cleanliness, predeposition sputter etches, and the proper energy and composition of the beam. We also see some evidence that oxygen impurity in the films may degrade their encapsulation properties, perhaps explaining the somewhat better results with the Si_3N_4, which is slightly more stable chemically compared to SiO_2 than AlN compared to Al_2O_3.

We wish to thank John Wager for the Auger results and Harry Wieder for several useful conversations. We also acknowledge the financial support of the U.S. Office of Naval Research (Contract N00014-76-C-0976), the Basic Science Program of Seoul National University, supported by USAID, the Scientific and Research Council of Turkey, and the faculty improvement program of Istanbul University.

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APPENDIX M

DEPTH AND CARRIER CONCENTRATION DEPENDENCE OF PHOTOLUMINESCENCE FEATURES IN HEAT TREATED GaAs:Si

Hülya Birey[a] and James Sites
Physics Department, Colorado State University
Fort Collins, Colorado 80523

ABSTRACT

The photoluminescence (PL) spectra of silicon doped n-type GaAs of four different carrier concentrations from 4×10^{15} to 3×10^{18} cm^{-3} were examined. Successive measurements as the samples were annealed for times from 15 to 60 minutes at 600-700°C, and as they were successively etched back, revealed that all PL changes were surface related, with a typical depth of 1 μm.

a) Permanent Address: Physics Dept., Istanbul Univ., Istanbul, Turkey

APPENDIX N

BROAD BEAM ION SOURCE OPERATION WITH FOUR COMMON GASES

S. Pak[a)] and J. R. Sites

Physics Department, Colorado State University
Fort Collins, CO 80523

ABSTRACT

A Kaufman-type broad beam ion source, used for sputtering and etching purposes, has been operated with Ar, Kr, O_2 and N_2 gas inputs over a wide range of beam energies (200-1200 eV) and gas flow rates (1-10 sccm). The maximum ion beam current density for each gas saturates at about 2.5 mA/cm^2 as gas flow is increased. The discharge threshold voltage necessary to produce a beam and the beam efficiency (beam current/molecular current), however, varied considerably. Kr had the lowest threshold and highest efficiency, Ar next, then N_2 and O_2. The ion beam current varied only weakly with beam energy for low gas flow rates, but showed a factor of two increase when the gas flow was higher.

APPENDIX O

SPUTTER DAMAGE IN GaAs EXPOSED TO LOW ENERGY ARGON IONS

H. E. Schmidt, P. E. Jensen, and J. R. Sites
Department of Physics, Colorado State University
Fort Collins, Colorado, 80523

ABSTRACT

Substrates of n-type GaAs were exposed to charge neutralized argon ion beams of uniform energy ranging from 50 to 500 eV. Exposure times were 10-30 minutes with a beam density of 1 ma/cm^2. Schottky barrier diodes were formed on the sputtered surfaces using gold films. Capacitance and current measurements showed a marked decrease in barrier height for samples sputtered above 150 eV, though rectification persists to higher beam energies. Chemical etching of the damaged layer to restore the Schottky barrier height showed that the characteristic depth of heavy damage was 20-50 A, increasing with ion beam energy.

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